Eventide
the next step

BD 955

BROADCAST DIGITAL AUDIO DELAY LINE

INSTRUCTION MANUAL

EVENTIDE INC. • ONE ALSAN WAY • LITTLE FERRY, NEW JERSEY 07643 • 201-641-1200 • TWX: 710-991-8715

LIMITED WARRANTY

ALL EVENTIDE EQUIPMENT IS WARRANTED FOR A PERIOD OF ONE YEAR

from the date of purchase from Eventide or an authorised dealer, against defects in material or workmanship. In case of difficulty, consult Eventide or your dealer for instructions.

This warranty does not apply to mechanical defects caused by use or rough handling, or to damage caused by improper operation not in accordance with this manual. Cause of defect is in the sole judgement of Eventide. There are no other express or implied warranties, and no warranty of merchantability or fitness for a particular purpose.

The warranty is voidable at Eventide's option under the following circumstances:

- if the equipment is connected to an improper voltage supply.
- if the user makes unauthorized modifications of any type. If such modifications are made, user agrees to pay for any time or parts necessary to remove the modification before repair.

Eventide will under no circumstances be responsible for consequential damages caused by failure of equipments of its manufacture, or for any other reason. Our sole liability is for repair or replacement of defective parts, under the terms of the warranty.

SHIPPING

Equipment should be returned, if possible, in the original packing container. Loose cards must be wrapped in conductive foil (damage caused by failure to do this will render the warranty void). If the original container is not available, the equipment must be packed to prevent damage from crushing or dropping. Damage caused by inadequate packing for service return is not covered by warranty. We recommend shipping via UPS rather than by US mail, and air freight if you are in a hurry. If in our opinion the packing container is inadequate for return shipment, we reserve the right to supply a new container and charge for same.

The warranty covers return shipping in the continental US except Alaska. Return shipments will not be insured unless the customer requests and agrees to pay for same. If a more expensive form of shipment is requested, customer will be charged for same.

ALL RETURNED UNITS, IN OR OUT OF WARRANTY, MUST BE PREPAID TO OUR DOOR.

ALL RETURNED UNITS MUST BE ACCOMPANIED BY A COMPLETE TROUBLE REPORT, DETAILING ALL THE PROBLEMS EXPERIENCED, CONDITIONS OF OPERATION, ETC.

FOREIGN SHIPMENTS

Foreign shipments must be returned fully prepaid, including Customs and brokerage charges. Repaired equipment will be shipped all charges collect. A commercial invoice stating 'goods of US manufacture - being returned for repair' and giving a fair market value of the unit should accompany the shipment, to save time and expense. A copy of this invoice should also be mailed to Eventide.

REPLACEMENT OF PARTS UNDER WARRANTY will be done free of charge provided that the defective parts and the warranty card for the unit are received by Eventide.

WARRANTY REGISTRATION FORM
MODEL BD955 DIGITAL DELAY LINE

SERIAL NUMBER_____ DELAY 6.4SEC ( ) 3.2SEC ( ) 1.6SEC ( )

BANDWIDTH 7.5kHz ( ) 15kHz ( ) STEREO MASTER ( ) SLAVE ( )

DATE PURCHASED_____

YOUR COMPANY_____

ADDRESS_____

CITY/STATE/ZIP_____

STATION CALL LETTERS_____ AM ( ) FM ( )

STATION CALL LETTERS_____ AM ( ) FM ( )

CHIEF ENGINEER'S NAME_____

Person to whom data should be sent if different from Chief Engineer_____ TITLE_____

Site where equipment will be located if different from above_____

_____

Is this site the studio? ( ) transmitter ( ) both ( )

From whom did you purchase this delay line? FACTORY? ( ) DISTRIBUTOR/REP? ( )

If distributor, please give name and location_____

_____

How did you learn about this product?_____

Additional space for comments if desired. Thank you.

* * * *

Please check if you would like information on other Eventide products:

H969 Harmonizer®( ) H949 Harmonizer®( ) H910 Harmonizer®( )

SP2016 Signal Processor ( ) JJ193 Delay Line ( ) 2830 Omnipressor®( )

RETURN FORM TO:

EVENTIDE INC. • ONE ALSAN WAY • LITTLE FERRY, NEW JERSEY 07643 • 201-641-1200 •

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INTRODUCTION

The BD955 Broadcast Digital Delay Line is designed to enable the broadcast licensee to meet his obligation to the public and to the regulatory authorities to prevent obscene and/or libelous material from being transmitted over his facilities. It does this by automatically delaying program material by up to 6.4 seconds, thus allowing time for the monitoring operator to make the decision as to whether the material being delayed fits in either category.

If it does, either of two methods may be used to ensure that material is not aired. The first of these methods is standard: A taped jingle, censor's beep, or announcement is placed on the air and the delay line output is temporarily cut off. The second method is unique: newly developed electronic circuitry (patent pending) allows the entire contents of the delay to be "dumped", and the program resumed without interruption. Auxiliary circuitry can be used if desired to prevent uncontrolled sources (such as telephone callers) from being aired until the delay is again long enough to provide protection.

Additional features of the delay line include the ability to generate short delays for use in audio production applications, and to synchronize audio and video in cases where video is transmitted via satellite and audio via landline.

When compared to the traditional method of delay using tape loops, cartridges, or even two recorders with the tape stretched between them, the BD955 exhibits greater reliability, better and more consistent quality, no requirement for operator attention, and, in cases where it is used continually, lower monetary cost compared to that of a high quality tape machine that would be otherwise unavailable. Of course, the unique variable delay capabilities used in the "catch up" mode are mechanically unobtainable, as are the short delay times so useful in production and synchronization applications.

This instruction manual covers use, principles of operation, technical data, and contains alignment and troubleshooting data should this be required. We have also reprinted a copy of the "blurb sheet" for your convenience. May we take this opportunity to thank you for purchasing this Eventide unit, and to encourage you to return the warranty sheet. This will permit us to furnish corrections and updates, as well as possible application notes and future product announcements. If you have any questions or comments we should be pleased to hear from you.

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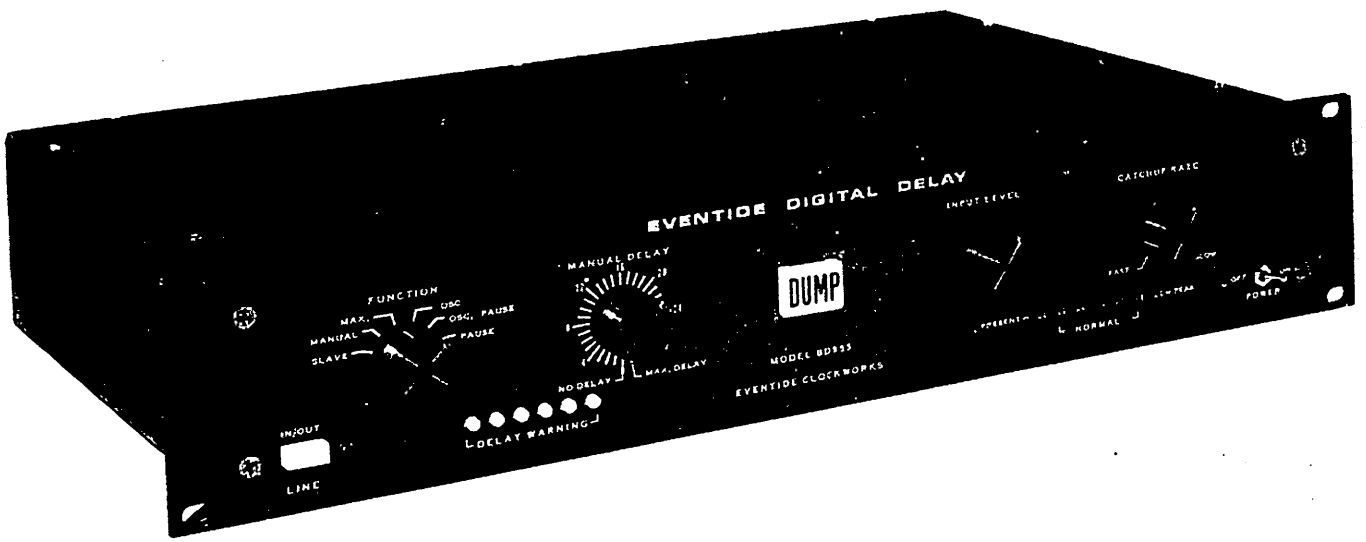
BROADCAST DIGITAL AUDIO DELAY LINE

MODEL BD955

THE DIGITAL BROADCAST DELAY LINE THAT BREAKS MURPHY'S LAW!
No tape loops that snap. No moving parts that break. No dead air.



The Eventide BD955 broadcast digital audio delay line offers memory capacity to delay signals up to 6.4 seconds. It also incorporates a unique "catch-up" feature, which eliminates the need for a taped jingle or announcement.

EXCLUSIVE CATCH-UP MODE

With the BD955, it's easy to get in and out of delay operation. After pressing the DUMP button, an exclusive mode of operation allows the program to continue in real time, without the necessity for filling the delay period with a jingle or announcement. Instead, as the DUMP button is depressed, the delay goes to zero, and the obscenity is deleted. Then, the delay increases at a variable rate while the program is continuing, so that a new delay margin for deletion is built up. This catch-up mode does not introduce wow, and is virtually undetectable in operation. A front panel display shows, in digital form (a progression of lighting LED's), how much margin the announcer has. Until the delay is fully restored, he will have to be more alert, but the mode permits much faster resumption of the program, without false interruptions. The catch-up mode may be defeated if normal delay operation is required.

A VALUABLE PRODUCTION TOOL

When not being used as an editing delay, the BD955 delay line may be used as a production tool. Front panel switches allow setting the delay from about 6.5 milliseconds to the unit's maximum delay, a range useful for many production effects, including so-called 'doubling', or giving the audible illusion of multiple speakers, singers or instrumentalists.

FULL BANDWIDTH PERFORMANCE

A multi-LED level indicator promotes proper level setting for maximum dynamic range. The standard unit provides full 15 kHz frequency response. For applications where wide band frequency response is not needed, such as the delaying only of 'phone signals, the user may opt for a 7.5 kHz model, at substantial cost saving.

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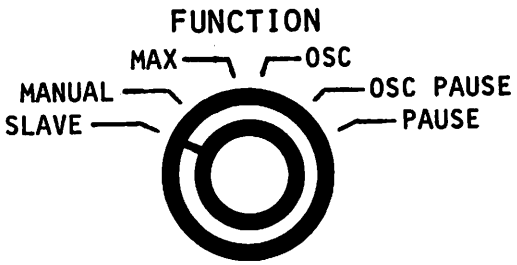
MODEL BD955 BROADCAST DIGITAL DELAY LINE

specifications:

INPUT CHARACTERISTICS	Impedance nominal 10 k, balanced, maximum level +24 dBm. Full dynamic range from 0 to +22 dBm levels. XLR female connectors.
OUTPUT CHARACTERISTICS	Electronically balanced, maximum level +22 dBm into 600 ohms. XLR male connector.
DISTORTION	Less than .3% at 1 kHz, reference level.
DYNAMIC RANGE	Greater than 90 dB from clipping to noise floor.
DELAY	Memory capacity 3.2 or 6.4 seconds. Front panel switch allows delay setting from about 6 ms to maximum.
FREQUENCY RESPONSE	15 kHz ± 1 dB or 7.5 kHz ± 1 dB
SIZE	Requires 8.89 cm (3½ ") x 48.26 cm (19") panel space. Extends 31.75 cm (12½ ") behind panel.
POWER REQUIREMENTS	115 VAC, 50-60 Hz, or 230 VAC, 50-60 Hz. Nominal power dissipation 40 watts.
REMOTE CONTROL	Control of the DUMP switch and indication of delay margin provided on the rear panel connector. Relay contact closure indicates manual DUMP activation.

NOTES:

- ★ *The pricing of the BD955 Broadcast Digital Delay Line is largely dependent upon the product of frequency response and delay. The customer is urged to consider his requirement carefully.*
- ★ *For other frequency response or delay, request quotation.*
- ★ *Once a unit has been purchased, it is possible to alter the maximum delay time with little trouble. IT IS IMPRACTICAL TO CHANGE THE FREQUENCY RESPONSE.*
- ★ *STEREO CONNECTION for two units is available at a small extra charge. This allows either unit to be used as mono backup.*



The FUNCTION control determines the mode of operation of the BD955 delay unit. Its six rotary positions operate as follows:

SLAVE: Configures the delay line to receive delay change commands from another BD955. In this mode, the cable provided with a master/slave combination must be connected to both units. Both DUMP switches are connected in parallel, and activating either is equivalent to pressing both simultaneously. After the delay is reset by the DUMP button, the delay of both units will increase synchronously. IMPORTANT NOTE: SLAVE operation does not transfer the MANUAL control setting from one unit to the other. If it is desired to operate the master unit in the MANUAL mode, the SLAVE must also be in MANUAL, and both MANUAL DELAY controls should be set identically.

MANUAL: In this mode, the MANUAL DELAY control determines the delay setting of the unit. Refer to the MANUAL DELAY control description for information on settings.

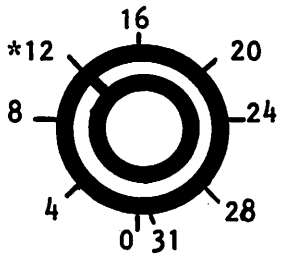
MAXimum: Setting the FUNCTION switch to this position assures that the catchup rate will be as fast as permitted by the internal timing. This position is equivalent to the rate obtained by setting the unit to OSC with the catchup rate at maximum, or to PAUSE operation with no input signal.

OSCillator: In this position, the catchup rate is determined by an internal oscillator. The speed of the oscillator is determined by the CATCHUP RATE control. Because signal characteristics are not taken into account, operation of the oscillator will be more obtrusive than use of the PAUSE mode.

OSC PAUSE: This mode is a combination of the oscillator and pause modes. It is used primarily to assure that catchup will occur even with continuous program material. In operation, catchup will occur at the oscillator rate if no pauses occur, or faster (and less obtrusively) if they do.

PAUSE: This mode causes the delay to increment whenever the input signal drops below a certain threshold. Thus, delay is increased during syllabic pauses in speech or silent periods in programming. Because these pauses occur during low signal intervals, this mode is the least obtrusive.

MANUAL DELAY

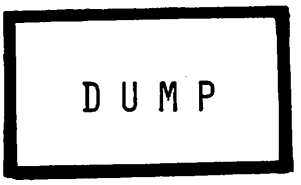


MANUAL DELAY CONTROL

When the FUNCTION switch is in the MANUAL position, the delay is determined by the MANUAL DELAY control. This is a 32 position rotary switch with no stop, so that it may be continuously rotated. No calibrations are included on the front panel because the delay is not only a function of the switch setting, but also of the options (delay/frequency response) purchased. The table below shows the approximate delay obtained at each switch setting.

Note three special positions:
Position 0 is always zero delay.
Position 31 is always maximum delay.
Postion 12 is the closest approximation to the round-trip delay time by a video signal transmitted to a geosynchronous satellite. This permits an audio signal transmitted by landline to be delayed conveniently so that audio and video may be synchronized.

SWITCH SETTING	15KHZ UNITS DELAY TIME 6.4SEC	3.2SEC	1.6SEC	7.5KHZ UNITS DELAY TIME 6.4SEC	3.2SEC	1.6SEC	MAX. DELAY
0	0	0	0	0	0	0	
1	6.25	6.25	6.25	12.5	12.5	12.5	milliseconds
2	12.5	12.5	12.5	25	25	25	
3	18.25	18.25	18.25	37.5	37.5	37.5	
4	25	25	25	50	50	50	
5	56	56	56	62	62	62	
6	87	87	87	125	125	125	
7	118	118	118	137	137	137	
8	150	150	150	150	150	150	
9	181	181	181	162	162	162	
10	212	212	212	175	175	175	
11	244	244	244	237	237	237	
12	275	275	275	250	250	250	
13	306	306	306	262	262	262	
14	387	362	337	375	325	325	
15	469	418	369	437	387	337	
16	525	450	375	450	400	300	
17	631	506	431	562	462	412	
18	737	587	487	675	575	425	
19	894	694	545	837	637	487	
20	1025	750	575	950	700	500	
21	1.20	.881	.631	1.16	.81	.562	seconds
22	1.43	.987	.687	1.37	.975	.675	
23	1.69	1.14	.768	1.64	1.08	.737	
24	2.00	1.27	.825	1.90	1.20	.750	
25	2.36	1.45	.906	2.26	1.41	.862	
26	2.79	1.66	1.01	2.73	1.63	.975	
27	3.29	1.89	1.12	3.23	1.89	1.09	
28	3.87	2.15	1.20	3.80	2.10	1.15	
29	4.58	2.46	1.33	4.51	2.41	1.26	
30	5.41	2.79	1.46	5.37	2.77	1.43	
31	6.4	3.2	1.6	6.4	3.2	1.6	



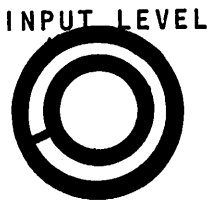
DUMP CONTROL: This momentary push button switch initiates the deletion of program material in the following manner:

1: When the DUMP switch is depressed, the delay instantly goes to zero. It will remain at zero as long as the button is held in. An internal relay closes when the switch is pressed, and opens about 1/2 second after the switch is released.

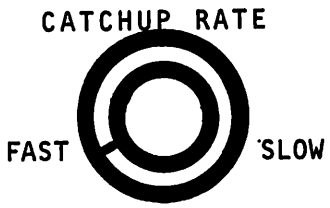
2: When the DUMP switch is released, the delay will increase according to the setting of the FUNCTION control.

3: Depressing the DUMP switch again before the delay has reached maximum will cause the delay to go to zero.

There is a potential conflict between the MANUAL DELAY control and the DUMP switch: When DUMP is depressed, the delay will go to zero regardless of the MANUAL DELAY setting. However, when the DUMP switch is released, the delay will immediately assume the MANUAL setting, if the FUNCTION switch is in the MANUAL position.

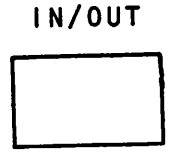


INPUT LEVEL: This control is a continuously variable attenuator which allows setting the unit to optimum operating level. The section on INPUT LEVEL SETTING gives criteria for proper adjustment of this control.



CATCHUP RATE: This control determines the rate of delay increase in the OSCillator mode, and the minimum rate of delay increase in the OSC PAUSE mode. When fully counterclockwise, the catchup rate is maximum. When the control is fully clockwise, the rate is quite slow, and several minutes are required to achieve full delay.

POWER ON/OFF: Placing this switch in the ON position applies AC power to the delay line. When power is applied and the unit is not in the MANUAL DELAY control mode, the delay is initialized to zero to prevent transients caused by reading invalid data from memory.

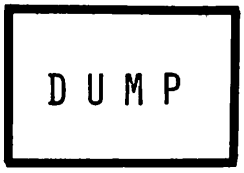


LINE IN/OUT: Depressing this control applies audio to the delay line, and enables its output. When it is OUT, there is a DC path from the input to the output, and power need not be applied.

FRONT PANEL INDICATORS

IN/OUT LAMP: This LED is associated with the IN/OUT switch. When this switch is in the IN position, the LED becomes illuminated, signifying that the delay unit is IN line.

DELAY WARNING indicator group: These two color LED's advise and warn the operator how much delay margin the delay unit has built up. When the DUMP button is depressed, all six indicators turn red and flash periodically. This signifies that the delay is at or near zero and it is unsafe to place the phone caller on the air. As the delay time increases, the flashing red indication stops and the indicators, starting at the left, turn green. The number of indicators which have turned green show graphically how much time there is to edit the incoming program. One advantage of this indicator is that it is much easier to interpret than a digital readout. When one or two green lights are on, the operator knows that he must be especially alert; when they're all on, there's plenty of time to react. This feature allows resumption of program sooner than would otherwise be the case.



DUMP SWITCH LAMP: The incandescent lamp in this switch may be used in conjunction with the DELAY WARNING indicators: An internal jumper selects the drive point for this lamp so that when a selected green LED comes on, so does the DUMP lamp. This feature can be used to relieve the operator of judgement. He can be told "reactivate the 'phone when the light comes back on". Alternatively, the voltage controlling the lamp can be used to control the internal relay so that this relay disables the telephone during the period involved, thus preventing any possibility of human error.

SIGNAL LEVEL INDICATOR GROUP: These LED's function as a "bar graph" display which depicts peak audio input levels. The leftmost "PRESENT" indicator becomes illuminated when a small amount of signal is present. The PEAK indicator comes on when the digital system is on the verge of instantaneous clipping. The section on INPUT LEVEL SETTING describes this indicator and the associated INPUT LEVEL control.

INPUT LEVEL SETTING

The BD955 Digital Delay Line is similar to amplifiers, equalizers, tape recorders, transmitters, and virtually every other electronic device with the possible exception of a piece of wire at absolute zero in that it has a certain, limited, dynamic range. Dynamic range is defined as the levels between which operation of the device in question is useful or acceptable. As a practical matter, the range is usually bounded on the high side by excessive distortion, and the low side by excessive noise. In many equipments, a level indicating device such as the familiar VU meter is provided to indicate when the unit is operating at the proper level. A tape recorder, for instance, has a certain percentage of distortion at 0VU, and this percentage rapidly increases as the signal level increases. The noise level is some number of decibels below 0VU. The number of decibels between distortion and noise is defined as "dynamic range".

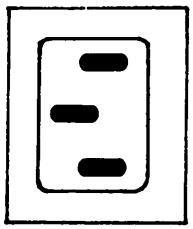
Signal sources typically have a dynamic range much greater than that of electronic devices. Likewise, the ear can hear a dynamic range much greater than that of electronic devices. Since the electronic device is the limiting factor, it is obviously a good idea to set the operating level of the delay line to take advantage of the maximum dynamic range of which it is capable. This is the equivalent of making sure that the meter on a tape recorder is reading around 0VU most of the time.

To enable accurate setting of input level, a row of solid state indicators form a "bar graph" display underneath the INPUT LEVEL control. The lamps are graduated in level so that, with any significant input signal, the leftmost becomes illuminated, and, when the entire group is on, a clipping condition exists. With the INPUT LEVEL control fully clockwise, clipping will occur at about +6 dbm at 1 KHz. This typically corresponds to approximately 0VU in most facilities. Of course some margin above 0VU is required and consequently the INPUT LEVEL control will normally be operated between 12 and 3 o'clock.

The "ballistics" of the level display are such that it responds to instantaneous peaks. This fact, coupled with internal circuitry designed to reduce internal system gain as input level increases ("companding"), makes it desirable to operate the unit with the rightmost indicator flashing periodically. Such instantaneous peaks will generally be inaudible. The exception to this rule is when the delay line is connected in the audio chain following compression and limiting: in this case, the INPUT LEVEL should be set so that the second rightmost lamp is flashing frequently, and the rightmost virtually never.

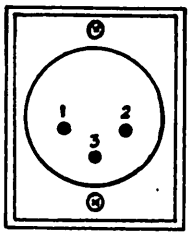
As the dynamic range of the delay line is about 90db, following this procedure will insure that it is not the factor limiting performance of even the widest dynamic range stations.

REAR PANEL CONNECTORS

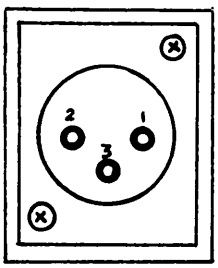


AC POWER CONNECTOR: This connector accepts an internationally approved "IEC" connector. The line cord furnished with the unit is for United States standard 3 wire outlets. The line voltage is specified on the serial number plate, and may be changed from 115VAC to 230VAC by a simple internal wiring change.

FUSE HOLDER: The fuse in this holder is in the primary circuit of the power transformer. It should be replaced only with a 1/2 amp slo blo (115VAC) or a 1/4 amp slo blo (230VAC).



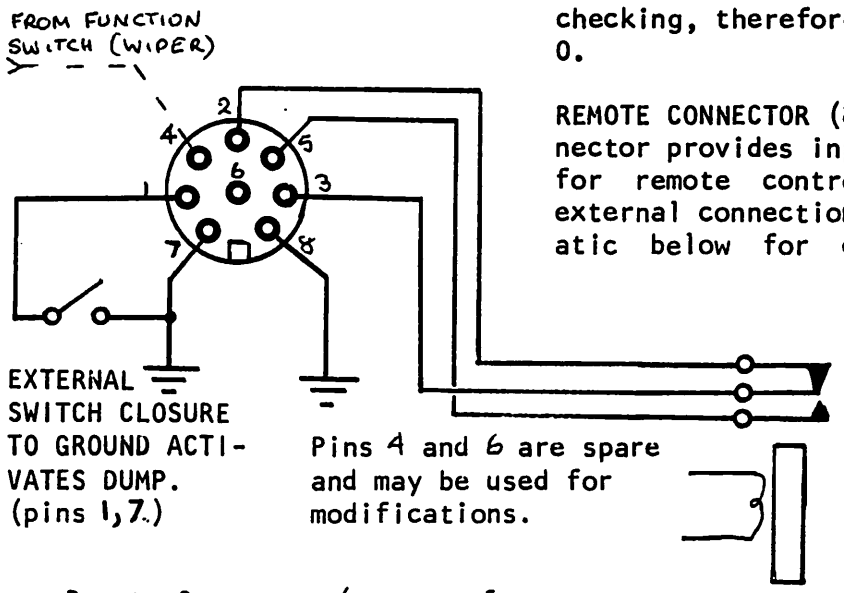
OUTPUT CONNECTOR (3PIN XLR MALE): This is the audio output connector for the delay line. Refer to the specifications for levels and impedances.
PIN 1 is shield/chassis ground.
Pin 2 is output -phase.
Pin 3 is output +phase.



INPUT CONNECTOR (3PIN XLR FEMALE): This is the audio input connector for the delay line. Refer to the specifications for levels and impedances.
Pin 1 is shield/chassis ground.
Pin 2 is input -phase.
Pin 3 is input +phase.

NOTE: For both input and output, the signal phase is arbitrary except at the very shortest delays, as many wavelengths of any given signal will be in the delay at any time. For phase checking, therefore, the delay should be set at 0.

REMOTE CONNECTOR (8 PIN DIN FEMALE): This connector provides input and output connections for remote control of the DUMP switch and external connection to the relay. See schematic below for connection.



Remote Connector (as seen from behind the unit).

IMPORTANT NOTE: This drawing is a REAR PHYSICAL VIEW of the plug. The numbers molded on the plug should be ignored as they are both illogical and do not correspond when supplied by different vendors.

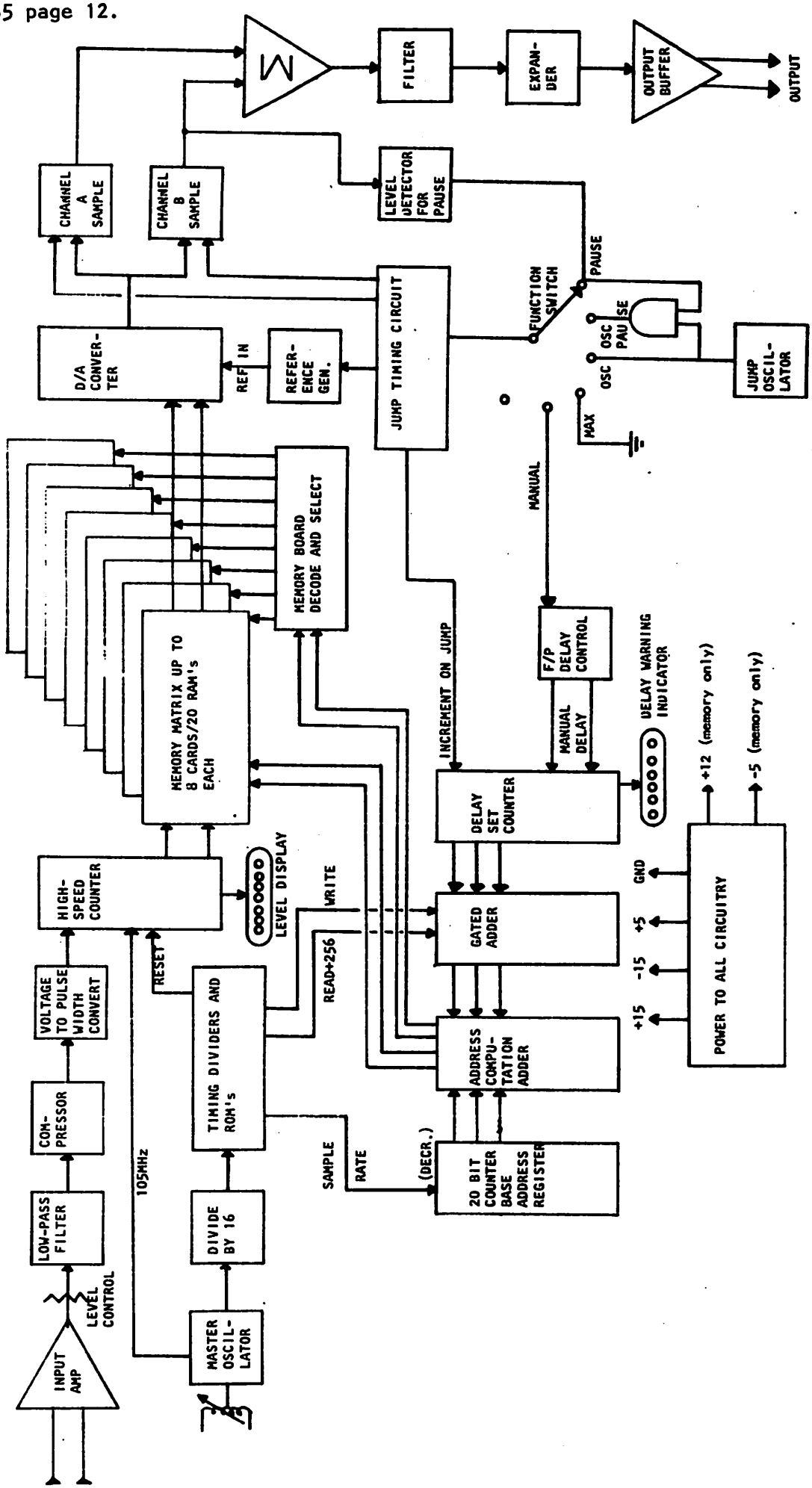
When wiring the plug, connect your circuitry to the pins corresponding to the physical position shown on this drawing.

SYSTEM INTERCONNECTION

The BD955 may be used in a straight delay mode, or one may take advantage of the catch up mode. If it is being employed to replace an existing tape delay, it may be connected in the system identically to the tape unit, i.e., substitute the delay input and output connectors for the tape system input and output connectors. In this mode, the delay should be set to maximum and the DUMP switch never touched. Whatever control system currently exists may then be used without modification.

If this is a new installation, and you wish to have the versatility of the catch up mode and the use of fixed delay as well, there are several connection schemes and control methods that may be used, and other commercial or easily produced devices which will permit both.

BD955 BROADCAST DELAY LINE
ELECTRONIC BLOCK DIAGRAM



The purpose of this section is to describe in a fairly specific manner the method by which the delay line operates. The various circuit sub-groups are dealt with individually, with reference to what each one does and how it does it. To make this section of a manageable length, we assume that the reader is familiar with the individual integrated circuit "building blocks", and so will describe the IC's place in the scheme of things rather than the operation of the IC itself. Pin connections and brief descriptions of the IC's will be found at the end of this manual.

The circuitry of the BD955 Digital Delay Line is contained on three printed circuit assemblies. They are:

B955 Rev.- Main circuit and mother board
B951 Rev.- Random Access Memory board (B951 boards not used in units with s/n 95758 & above)
303C Rev.- Compressor/Expander boards (See page 24)

The only electronic components not on these boards are the +15 volt DC regulator (mounted on the right side of the chassis), the +5 volt DC regulator, (mounted on the rear of the chassis), and the power transformer. The various input, output, power, and control connectors are also located on the chassis. Six schematic drawings reference these assemblies, and should be referred to as an integral part of this section.

The power supply (schematic sheet #5) generates the regulated DC voltages required by the remainder of the circuitry. Full-wave bridge rectifiers generate raw DC at about +10V for the 5 volt supply, and at +/- 20 volts for the +15 regulated and -15 regulated supplies. The raw DC is regulated by IC regulators, mounted on the chassis in the case of the +5 and +15 supplies, and on the circuit board in the case of the -15 supply. Three silicon diodes in series with the +15 supply provide the 12 volts required by the memory array, and a zener diode/pnp transistor regulator provides the -5V (at very low current) required as bias for the memories. The 5V is employed by the digital logic as a power supply and, after filtering, as a bias supply for the analog circuitry. The + and - 15 volt supplies are used by the analog circuitry and output amplifiers.

TIMING OSCILLATOR:

IC33, sheet #2, a high-speed emitter-coupled oscillator provides basic timing for the system. All clocks are derived from this signal by various dividers and counters. This oscillator operates in the 100MHz range and there exists a possibility for interference if the delay line is mounted in close proximity to an FM tuner. If this should occur, it is permissible to retune the oscillator slightly without adverse effects on the rest of the unit. The output of the oscillator is applied to IC-34, a low power divide by 16 circuit, and to the input of the first counter in the analog to digital (A/D) converter.

TIMING CHAIN: The output of the divide by 16 counter is connected to the synchronous timing generator consisting of IC's 47 through 52, and IC 54 (sheet #1). IC's 47 and 50 divide the 6MHz output of IC34 by an additional factor of 16 (IC 47) times 10 (IC50). The outputs of the these two IC's are decoded into unique time slots by read-only-memories (ROM's) IC-48 and IC-51, so that events can be initiated at the proper times. The ROM's are asynchronous, and latches IC-49 and IC-52 are used to "deglitch" the ROM outputs and apply the signals to the rest of the system. IC-54 is a flip-flop synchronously set and reset whose period is a few 100MHz cycles shorter than the maximum count of the A/D converter, and whose output enables the A/D counter. This circuit effectively prevents overflow of the A/D. The inter-relation of the timing signals produced by this circuitry is shown in the timing diagram.

ANALOG/DIGITAL CONVERTER

The Analog to Digital converter changes the analog input signal into the discrete voltage levels required for storage in the digital memory. This is accomplished by "sampling" the input signal at a fixed interval (determined by the timing circuitry described above) and measuring the voltage of the sample. The process is as follows: (refer to schematic sheet 2)
1: The input signal is applied to IC-43 pin 8 at all times. IC-43 is a quad CMOS analog switch. During the "sample" interval, the .0039uF capacitor is charged to the voltage of the input. When the sample pulse is turned off, the capacitor is linearly discharged by a current sink. The discharge time is a linear function of the initial voltage. Comparator IC-44 detects when the voltage on the capacitor reaches 0 volts. IC-29 is a gate which enables counter IC-32 during the period between the end of the sample pulse and the time when the capacitor voltage reaches zero. This time is proportional to the instantaneous voltage present on the capacitor at the end of the sample pulse, and is measured by the counter chain IC-30, 31, and 32. Each successive stage of the counter divides the previous input by two. The maximum count period, determined by IC-54, is just nanoseconds less than that required for the counter to reach a count of 2048, or 2 to the 11th power. Thus the A/D converter is capable of resolving "11 bits", which corresponds to an instantaneous dynamic range of about 66db. The outputs from the counter form the data word written into the memory under control of the timing circuitry.

The front panel level indicator is operated directly from the A/D converter: A 4 bit comparator, IC-28, compares the current value of the input signal with the state of the 4 bit counter IC-27. If the input signal is greater, then this new, larger value is strobed into the counter. If it is lower, the counter remains as-is. Thus, these two IC's form an instantaneous peak detector. The signal labelled "FLASH" is a slow speed clock which asynchronously decrements IC-27. This signal is orders of magnitude slower than the peak detection function. If no peak comes along, however, the counter slowly counts down. IC-26 is a ROM programmed to turn on various front panel LED's in response to the state of the decrementing counter. An additional output from the ROM inhibits the counter from going below zero and "wrapping around", thus causing repeated cycling of the level indicator.

INPUT SIGNAL CONDITIONING

Before reaching the A/D converter, the input signal must be conditioned. The conditioning includes compression which, with complementary expansion on the output, greatly increases the DDL dynamic range, and filtering, which decreases the amplitude of high frequency signals which could cause spurious responses from the DDL, known as "aliasing". The signal must also be offset to +5VDC, so that the converter, which is inherently unipolar, can convert AC signals. IC-46 comprises four operational amplifiers. The first section is a differential amplifier which provides a balanced input and large input voltage range. Following the LEVEL control comes a gain stage and two three pole low-pass filters to perform the anti-aliasing function. The compressor card has two sections, a voltage-controlled-amplifier (VCA), and a level detector. Unlike the normal compressor, these sections operate independently.

The input level is measured and fed to the VCA in such a manner that, for each 6db increase in input level, the gain of the VCA is decreased by 3dB. This provides a 2:1 compression ratio over a very wide dynamic range. The two .1uF capacitors and the resistors associated with this assembly are a high-pass filter to remove sub-audible frequencies (such as turntable rumble) from the input. The network between the compressor output and IC-45 allows biasing of the signal to +5volts as required by the A/D.

Ignoring the intervening delay circuitry temporarily, the output circuitry comprises a D/A converter and the associated circuitry required to change the digital numbers removed from the memory back to an audio signal. There are additional complications involved in this process, so we will discuss the normal mode first, and then show what happens during the "catch-up" mode.

IC's 35 and 36 are 6 bit latches which are strobed when each word becomes available at the memory output. This datum is applied to the input of D/A converter IC-37. This converter is a special type called a "4-quadrant multiplying" D/A. This means that the output current or voltage (in this case, current) is the product of the digital word and a reference voltage applied to the reference input pin 17. Assume temporarily that the reference is fixed at -10 volts. As each word is input, it is converted from a current output to an offset bipolar voltage by IC-41. The circuit constants are such that with a half scale digital input, the output voltage is 5 volts. As the input varies between zero and full scale, the output varies between 0 and +10V. (If the reference voltage is decreased, the offset remains the same but the full-scale amplitude decreases so that with a reference of 0, the output remains at 5 volts.)

After the voltage is available at the output of IC-41, it is sampled by IC-43, another analog switch identical to the one used in the input sampler. The output of this switch is amplified by IC-42 (pins 5,6,7) and then filtered as done in the input by a section of IC-45. This filtered signal is expanded in a fashion complementary to the compression performed at the input. I.e., the gain of the VCA is increased by 6db for each 6db increase in the signal level. This "companding" operation reduces by a factor of 2 the range of the signal going through the digital system and would theoretically give a dynamic range of over 120db. Noise pickup and other effects necessarily limit the improvement, but it is nonetheless quite dramatic. The output of the expander is applied to two sections of IC-45 which, together with their transistor buffers, comprise the output amplifiers. These circuits are of identical gain but opposite phase, so a quasi "balanced" output is available without response-degrading transformers. The peak to peak output level is also doubled. The output impedance is 300 ohms (150 ohms single ended), and suitable for driving any type of load. The 10 ohm resistors in the collector circuit decouple the buffer from the power supply and act as fuses if the output is accidentally shorted during test. (Shorting the output after the 150 ohm resistors is not harmful and can be endured indefinitely.)

THE CATCH-UP MODE

A unique feature of the DDL is its ability slowly and almost inaudibly to insert delay in live program so that time may be "caught up" without insertion of artificial pauses or putting extraneous material on the air. The key to this capability is the ability of the random access memory to look at various locations (delay times) upon instantaneous command. Each time a catch-up command "JUMP" is issued, the output of the delay line is displaced 256 samples, roughly 8 milliseconds, farther from the input, thus increasing the delay by that amount. This must be done as unobtrusively as possible. If it were done the obvious way, by reading in data at one rate and reading it out at another, slower rate, it would result in a continuous pitch shift which would abruptly terminate when the maximum delay is reached. This is unacceptable, so the jump method operates as follows:

Assume you are looking at a signal at time A and that you want to listen at time B, 8 milliseconds later: You can't simply switch times, because there would be an audible splice. This is the digital equivalent of splicing a tape without an angled cut. The digital equivalent of the 45 degree angle is synthesized using the previously unmentioned circuitry of the D/A section.

The output of the memory is actually sampled twice for each input sample. One sample reads the current value of the signal (sample A), and another sample reads the value 256 samples later. Normally, the second sample (sample B) is ignored by forcing the reference voltage on the D/A to be zero during the time the B data is in the latch. However, when the JUMP command is received, a counter, IC-40 is enabled. This counter, in conjunction with exclusive-OR gates IC's 38 and 39, forms a ramp generator which controls the reference voltage on the DAC. Normally, during sample A, the output is -10V, and 0 during sample B. As IC-40 increments, the A sample reference decreases to 0 and the B sample reference increases to -10V. Each step of the ramp occupies one sample period, so that the transition is not abrupt. Note that another section of switching IC 43 samples the B output. Both outputs are combined in IC-42 (pins 5,6,7).

The effect of all this is that, when a JUMP command is received, the amplitude of the current signal is decreased and the amplitude of the delayed signal is simultaneously increased. Because of the method of generation of the reference voltage, the sum of the two amplitudes is constant, thus providing a smooth transition (splice). At the end of the ramp interval, the counter is instantaneously reset, the A output incremented by 256 samples, and the B output disabled. Thus the next sample (at full amplitude) is equivalent to what would have been the next B sample. The B output is meanwhile ready for another increment.

CONTROLLING THE JUMP COMMAND

As smooth as the transition is, it is not inaudible. There will usually be some difference between the signals at the different times, and this will show up as a combination of phase and amplitude modulation of the output signal. This is sometimes unavoidable, but there is one further precaution one can take: If the JUMP takes place during a period of no signal, then there will be no splice "glitch".

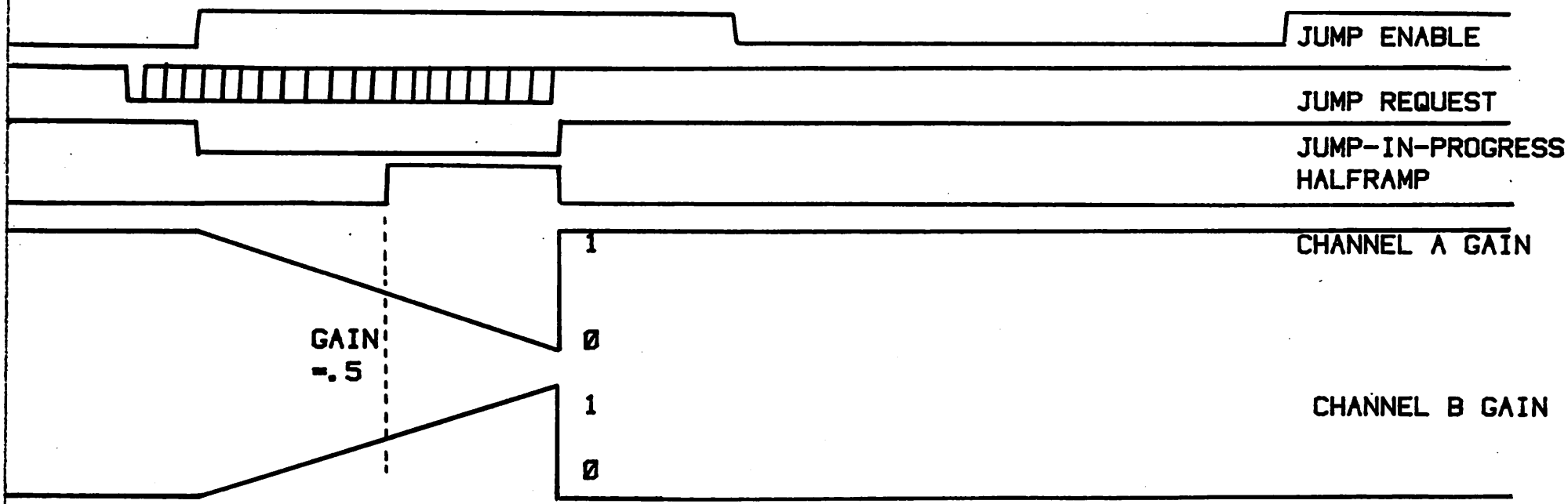
The major anticipated use for this unit is for changing delay during talk programming. Speech is characterized by many pauses, both syllabic and deliberate, for thinking, effect, or whatever. By carefully tailoring circuit time constants to these pauses, it is possible to add delay during natural pauses in speech. Splices so occuring are inaudible. The subjective effect, during catch-up, is that the speaker is talking a bit more slowly, but there is no pitch change and no distortion introduced! Additional catch-up modes are provided: If music programming, in which pauses are much less frequent, is contemplated, a variable rate oscillator can be used to initiate the JUMP command.

Because the pauses occur asynchronously with system timing, a bit of extra logic is required. Refer to sheet 1: When a JUMP command is received (NJREQ), a S-R flip-flop (IC-55) is set. Assuming that a JUMP has not occurred too recently, this request is passed through IC-53 (1,2,3) to IC-55 (8,9,10) which further qualifies the request by determining whether maximum delay has yet been reached, signified by a logic low at the FULL gate output. If it has not, IC-61 is set. This flip-flop enables the B output strobe. When a JUMP begins, the enable flip-flop, IC-54 is reset. This prevents another jump from occurring too soon. If this were not done, the jumps could be continuous and the output would be cut down to zero (catch-up rate same as real time passage). The maximum rate is thus determined by the input pulses to IC-59. Transition of the most significant bit on the ramp generator signifies the end of the jump, which permits the process to begin at the first jump request after the enable flop has been toggled.

The request rate is determined by the function switch. If the NJREQ line is grounded (MAX position), then jumps occur as fast as they are enabled. A relaxation oscillator (IC-60) can vary the rate substantially. In the OSC mode, the capacitor on the input of IC-60 is slowly charged through the front panel CATCHUP RATE control. When the capacitor reaches the threshold voltage determined by the resistor network connected to pin 3, pin 6 goes low, issuing the request. The digital circuitry then discharges the capacitor so that after the jump it must re-charge before a new request can occur.

The jump on PAUSE circuit works as follows: IC-56 amplifies the A output only. Its gain is controlled by a circuit board mounted trimpot, R1. (This adjustment can be changed to accommodate different talkers. IC's 57 and 58 form a dual threshold comparator. If the output from IC-56 crosses either threshold, the capacitor on the input to IC-59 is discharged through one of the diodes pointing to the comparator input. If there is a pause in the input signal, neither threshold is crossed, and the capacitor slowly charges through the resistor connected to +15V. When the capacitor voltage reaches the threshold of IC 59, again determined by the resistor network, a jump request is issued. In this case, the capacitor is not discharged by the digital circuitry, as we wish to take advantage of the pause as long as possible. The final mode, "BOTH", is a logical OR (a NAND gate is performing the OR function) of the PAUSE and OSC modes. In this case, if a pause occurs, the oscillator remains inactive, but if it doesn't, catch up is forced by the oscillator.

BD955 JUMP TIMING



When JUMP REQUEST (JREQ) goes LOW, a jump is initiated on the next JUMP ENABLE. If JUMP REQUEST remains low past the end of JUMP-IN-PROGRESS (JIP), an additional jump is initiated at the next JUMP ENABLE positive transition.

During a JUMP, the signal envelope is the sum of the signal multiplied by the channel A gain, and the signal delayed by 256 samples multiplied by the channel B gain. Because the signals may be in or out of phase (or in any phase relationship, for that matter), the signal envelope may have two partial nulls or one full null during the JUMP. If the signal is not a sine wave or other repetitive signal, this effect will be hard to observe, but audible nonetheless unless the PAUSE mode is in use.

Sheet 3 of the schematic diagrams contains the circuitry which actually controls the delay. The various counters and adders on this sheet determine the read and write addresses of the RAM, which contains data corresponding to the input data stream in consecutive order. The process works as follows:

WRITING DATA TO THE MEMORY

IC's 7 through 10 form a binary counter chain which is decremented every time a new word is written into RAM. The five chips have a count capacity of 2 to the 20th power, or about 1 million counts. The maximum capacity of the delay line is 1/4 of this, so the top two bits are ignored. Depending upon the card complement installed, fewer bits may be used. Each bit combination corresponds to one and only one address in the RAM array. The array uses 16K bit integrated circuits which have 2 to the 14th power storage locations. All chips get the bottom 14 bits applied to their address inputs. The next bit selects the individual row on the memory card, and the remaining (up to 3) bits uniquely select the card.

Once the A/D converter has completed a conversion, the data is placed on the memory DATA input lines (as opposed to ADDRESS lines, determined by the counter, above). This data is written into the addressed location, and the counter is decremented. On the next write command, a data word is written into the next (lower) memory location. This continues until the entire memory is filled, at which point the first location is overwritten with new data. The procedure can be likened to recording on a tape loop: When a point comes around again, whatever is present is erased and a new signal is impressed on the tape.

This write operation is performed at the sampling rate of the DDL. Thus, each address corresponds to an input sample. Since the counter, referred to as the "BASE ADDRESS REGISTER" is decrementing, it can be seen that looking at an address positively offset from the base address by a certain number of samples will show the same sample which was input that number of sample periods earlier. Thus, reading data from the memory +1000 samples from the register corresponds to a delay of 1000 sample periods (about 30 milliseconds).

The adders (IC's 11 through 13) accomplish this during READ operations. Note that one set of inputs to the adders is from the base address register. The other is from a group of AND gates whose inputs in turn are enabled by NWRITE. This means that the second input to the adders will always be 0 during write operations, forcing the write address to be equal to the base address. We shall refer to the read operations as READ A and READ B, depending upon the time slot during which they occur (and, of course the use made of the data). During normal operation (no jump request), READ A is performed as follows: The counter chain IC's 20 through 22 contains the fixed delay data. This is passed through the group of adders formed by IC's 17 through 19. Since all other inputs are grounded at this time, the adder output is identical to the adder input. This group of adders feeds its output through the AND gates to the first group of adders. Because the AND gates are now enabled, the read address equals the sum of the base address and the delay setting counter.

Thus the READ A operation retrieves data from the memory at the current delay setting the the DDL.

The READ B operation is identical, except that the +256 input of the adders feeding the AND gates is now enabled. The output of these adders is therefore the input (the current delay register) + 256, giving the B delay required when summed with the base address register. These are the only memory reference operations which occur in the DDL. Although dynamic memories are used, there is effectively no refresh requirement because all accesses are unconditional and sequential, thus guaranteeing that all row addresses are read in the required length of time.

One additional mode of operation is controlled by the memory logic circuitry: The delay register/counter group may be manually set, in addition to being incremented after each jump request. The NMANUAL line activates the PRESET inputs of the counters allowing front panel control of the delay. IC-24 is a ROM which controls the operation of the front panel LED's which indicate the current delay. These are RED/GREEN leds, and the polarity of the ROM output is such that when little or no delay is set, the lights all come on RED, while as delay increases, the lamps turn green sequentially. As an additional warning, the FLASH signal enables the ROM when the lights are red so that they flash on and off. The FLASH signal is derived from the base address register. The NFULL signal is provided to stop the delay counter from incrementing when the memory capacity of the unit is reached. NFULL is decoded by selecting the inputs to IC-23 with a PC board mounted DIP switch. To indicate FULL, all inputs must be 1's. If the corresponding switch is open, the input will automatically be 1. If the switch is closed, the gate waits until that bit in the counter is true.

The memory array decoding is performed by IC's 1, 2, and 6 (schematic sheet #4). 1 and 2 are address multiplexers and operate under the control of the timing ROM. Because 14 addresses are required for each memory IC, and size limitations preclude the use of 14 address pins on the package, the addresses are multiplexed. During the first portion of the memory cycle (RAS, or Row Address Strobe), the multiplexers permit A0 through A6, the least significant bits of the address, to be strobed onto the memory chip. The multiplexers are then switched to pass the next 7 bits (A7 through A13) to the IC. These are entered during CAS, or Column Address Strobe. The R/W (read/write) line is applied to all chips and determines whether the input data is to be stored, or whether output data is to be read. If a read operation is called for, data become available immediately (about 150 nanoseconds) after CAS. IC-6 decodes the board address implied by the output of the base address register and adder, and permits CAS to go to only the board which corresponds to the desired address. CAS strobes write data into the RAM, and enable the output buffers. For this reason, each RAM's input and output may be connected to the same line with no interaction.

The memory boards themselves contain two rows of memories and two TTL buffer chips. Thus all address and timing inputs present the system with a single load instead of the usual highly capacitive memory lines.

PLEASE NOTE: In units with s/n B95758 & Above, 8 cards is the equivalent of all four rows of 64K RAMs. 4 cards is equivalent to the top 2 rows of 64K RAMs. 2 Cards does not apply to newer units.

The one front panel control not discussed thus far is the "DUMP" switch (panic button). Refer to schematic sheet #1. This switch initiates the procedure whereby the data in the memory is effectively removed from the on-air program stream. It works as follows: Assume that the unit is operating at maximum delay, and one desires to delete the program material in the memory. Pressing the DUMP switch instantly zeroes the delay register. The DDL is brought back into real time, and data presently stored in memory is overwritten before the delay can catch up to it again. Simultaneously, a relay is closed for a variable period (depending upon purchase specifications). The relay is driven by a section of IC-62, a CMOS inverter with a very high input impedance. The input capacitor (pin 5) is rapidly discharged, and the transistor driver turned on. When the capacitor charges to the gate threshold, the relay is turned off. The lamp in the DUMP button (driven by another section of IC-62 and a transistor) may be used to indicate when a certain amount of delay has been recovered. The switch is interfaced so that a similar switch may be connected in parallel, contact for contact, to provide a remote control. The relay contacts are also brought to a connector, and may be used to short out audio from the offending source, or for any other control function. Depending upon purchase specifications, other interface options may be provided.

STEREO INTERCONNECTION

If so ordered, the BD955 may be provided with stereo interconnect facilities. When this is done, one unit acts as a master, and the other as a slave. The oscillator from the master provides the clock for the slave, and two logic signals, NJREQ, and NDUMP are cross connected to assure that the delays of both units remain identical. When two units are so connected, the operational characteristics of the second, "slave" unit differ from those encountered under normal operation.

When Master/Slave operation is desired, both units must be modified. This modification is relatively minor, and is normally provided by Eventide at the time of purchase. As mentioned in the Theory of Operation section, signals passed between the units are the master oscillator output, the jump request (which advances the delay) and the DUMP switch output. Electronic considerations require certain limitations on the slave unit to enable it to operate in this mode.

If a unit is designated as a slave, IT MUST BE CONNECTED TO ITS MASTER with the interconnecting cable provided to operate! This cable is quite short due to the high frequencies involved, and the units therefore must be mounted in the same rack, no more than about 7 inches apart. (The slave may be enabled to operate on its own in about 5 minutes, by undoing part of the modification. This requires opening the top cover and exchanging one socketed component for another.) For s/n B95857 & above, see page 22a for Master/Slave configuration.

When connected in the Master/Slave configuration, the following operating characteristics obtain.

1: The FUNCTION switch on the slave unit must be in the SLAVE position.
2: The INPUT LEVEL controls on both units remain independent.
3: All delay setting controls on the slave unit are ineffective.
4: The delay setting controls on the master unit affect only the master.
5: Pressing the DUMP switch on EITHER unit is equivalent to pressing the DUMP switch on BOTH units.

When the DUMP switch is pressed, both units will go to zero delay (unless the master is in a mode, such as MANUAL, in which the DUMP switch is ineffective), and then increase in delay according to the mode in which the master is set to operate. The slave will track the master in delay until delay reaches maximum, at which time, both units will stop at their final delay.

In the above discussion, it is assumed that both units are identical in terms of delay options. If the master and slave have different maximum delay capabilities, the unit with a greater delay will continue incrementing after the other stops. This is clearly undesirable because the whole purpose of stereo synchronization is to keep the channel delays equal. The way to avoid this problem is to set the dip switches at the input to the FULL gate identically in both units, and to a setting no greater than the maximum delay of the shortest unit.

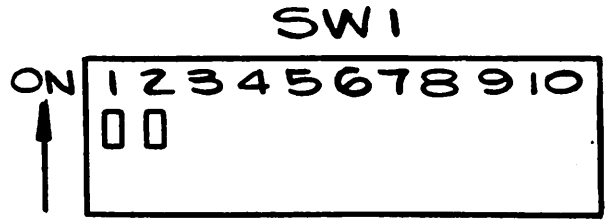
If the DUMP and catchup capability is not being employed, it is permissable to set both FUNCTION switches to the manual mode and set the delays identically. If this is done, the DUMP switch may still be used to trip the internal relay and control whatever external circuitry it may be connected to. However, it will have no effect on the delay of either DDL. (Again, both DUMP switches are wired in parallel so that pressing either is equivalent to pressing both.)

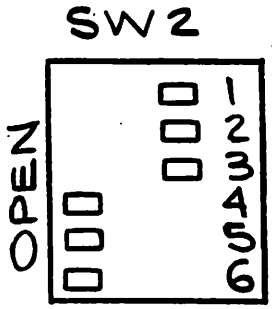
NOTE: This page is relevant for units with S/N B95857 and ABOVE. See page A-1b for exact switch locations on main board.

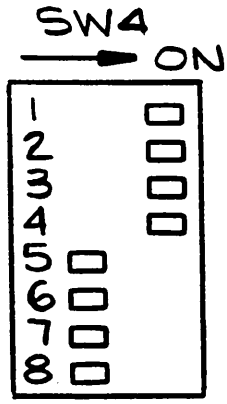
SWITCH CONFIGURATION

A. STANDARD (MASTER)

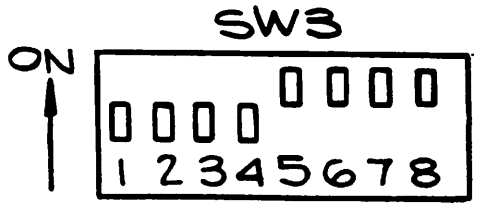
Standard and Master configuration are the same.



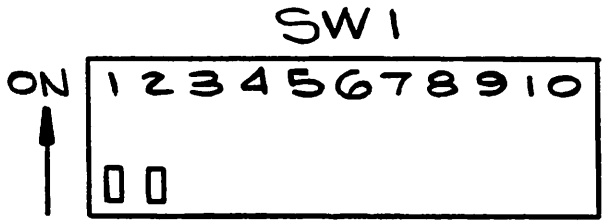


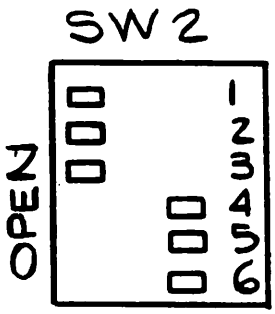


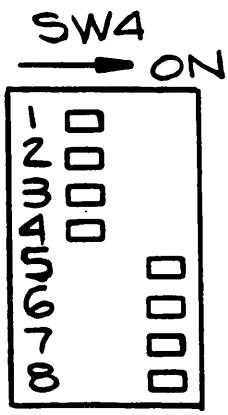
Note: Function switch on front panel can be in any position except "Slave".



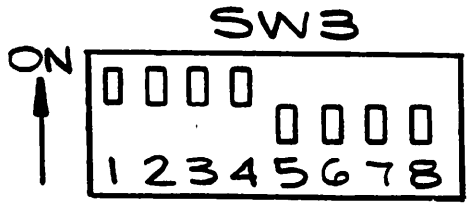
B. SLAVE







Note: Function switch on front panel should be in slave position.



INTERNAL ADJUSTMENTS AND ALIGNMENT PROCEDURE

There are several internal adjustments in the BD955. These are adjusted at the factory, and should not need readjustment or alignment. Some of these adjustments may be used to alter the operating characteristics of the unit, and as a convenience to the user are detailed here. All the adjustments are again mentioned in the alignment procedure.

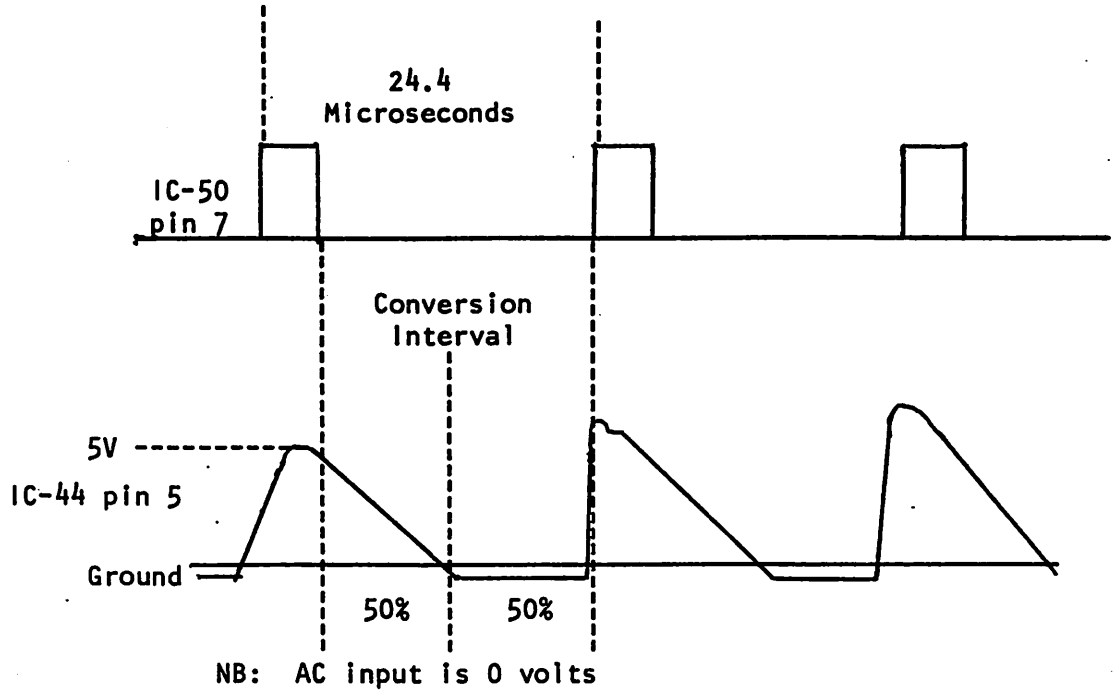
PAUSE LEVEL CONTROL: This is a single turn trimpot (R1) located on the main circuit board immediately to the left of the front leg of the right hand compander card (see parts location diagram). This control sets the threshold level of the PAUSE DETECTOR circuit, and is factory adjusted so that catch up will occur at a reasonable rate with normal speech. If desired, the threshold can be increased or decreased. Turning the control clockwise decreases the threshold, which means that a lower level signal will prevent a jump from occurring. This tends to slow down the catchup procedure, but makes it less audible. Turning the control counterclockwise increases the threshold, which speeds up the catchup rate, but makes the glitches more audible. The final setting is of course a compromise between long waiting and poor quality.

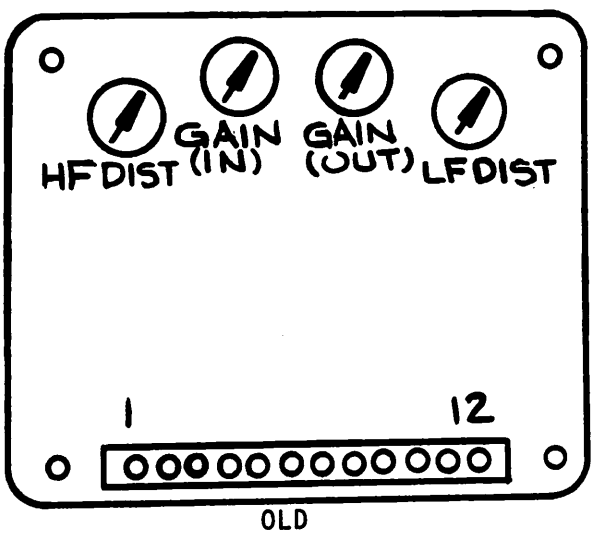
OSCILLATOR FREQUENCY: The master oscillator runs at about 104MHz to provide timing signals for the digital logic. Its frequency is controlled by an inductor on the far right side of the main circuit board and about half way back. (7.5KHz delay lines run at half this frequency.) Although the unit is well shielded, it is possible that enough spurious radiation may leak out to be picked up by an FM receiver located within a few feet. If your station happens to be on the same frequency as the master oscillator, and you are monitoring the air signal on an FM receiver a few feet from the DDL, and you pick up the master oscillator, you can either apply for a new frequency or retune the master oscillator. We suggest the latter. Slight changes (up to a few hundred KHz) will not affect the rest of the circuitry and no readjustment or realignment will be required. A plastic hex alignment tool or even a hex (Allen) wrench may be used, the latter carefully.

INPUT GAIN: This control is located on the left hand compander card (second control from the left looking at the card from the front panel). The gain of the delay line is factory adjusted to give full output with a +6dBm input signal with the INPUT LEVEL control at maximum. If this unit is being used at unusually low levels (for instance, with such "semi professional" equipment as TASCAM consoles and the like), it may be desired to increase the gain. This may be done by rotating the control clockwise. There is no reason why the gain would have to be decreased, as the INPUT LEVEL control handles this chore. Although the internal gain control has a very wide range, it should not be used to make up gain for which a preamplifier should be used, as the noise performance of the DDL will suffer. Increasing the gain by up to 10dB should have no material effect on the dynamic range.

OUTPUT GAIN: This control is located on the right hand compander card (third control from left, looking at the front panel). This control may be used to decrease the output level when feeding inputs which cannot handle +22dBm signals. Again, the control has a wide range, but large changes should be effected by a resistive pad rather than by this control.

A/D CONVERTER WAVEFORMS

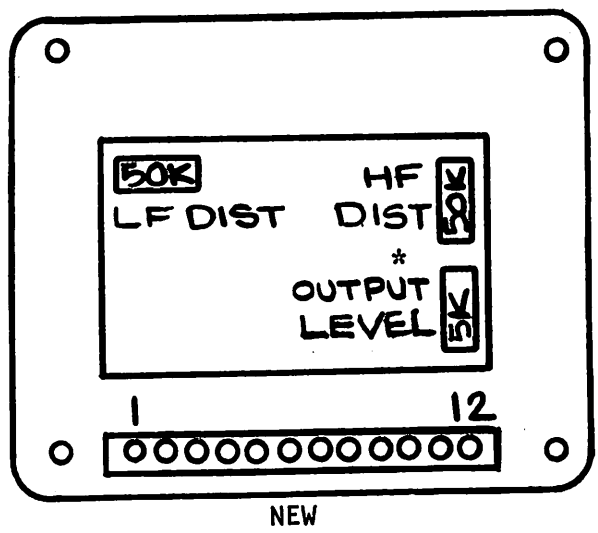




OLD

DBX 303 - CARDS USED AS COMPRESSOR OR EXPANDER

(INTERCHANGEABLE)



NEW

* Look for letter "E" or "D" on card.

"E" (Encoder) COMPRESSOR
"D" (Decoder) EXPANDER

THESE DBX CARDS ARE NOT INTERCHANGEABLE

The BD955 will have either two DBX 303 boards (interchangeable) or two DBX cards that act specifically as either a compressor or expander.

ALIGNMENT

Equipment required for alignment consists of a low distortion sine wave oscillator, a distortion meter or spectrum analyzer, and an oscilloscope. The oscilloscope should either be a dual trace unit or have an external trigger input.

OSCILLATOR FREQUENCY ADJUSTMENT: Note that this is not a critical adjustment unless for some reason you need exactly 6.4 seconds of delay! Any reasonable tolerance is OK, although a frequency counter may be used for precision. Attach the scope probe to pin 7 of IC-50. You should observe a 5V pulse waveform with a 1/5 duty cycle. Adjust the oscillator coil for a repetition rate of 40.96kHz, or a pulse period of 24.41 microseconds.

ANALOG/DIGITAL CONVERTER CURRENT SINK ADJUSTMENT: The control for this adjustment (R2) is immediately behind the rightmost control on the right hand compander card. Trigger the oscilloscope on pin 7 of IC-50 (same pin as last step). Adjust the scope so that falling edge of the pulse is at the left edge of the screen and the rising edge is at the right edge of the screen. The full screen corresponds to the conversion period. Adjust the gain of the other scope channel to 1 volt per division and with no input, put the baseline 1 division above the bottom of the screen. Now put the scope probe on pin 5 of IC-44. (Note: use a good scope probe. A high capacitance cable can disturb this measurement.) Adjust the sink current control so that the sawtooth signal on the screen crosses the center horizontal division of the scope screen at ground level (1 vertical division up).

NOTE: For all analog adjustments following, set the DDL in manual for zero delay. The distortion meter should have its high frequency cut filter IN.

INPUT COMPANDER: This is the left compander plug-in circuit card. Apply a 1kHz, +6dbm signal to the input of the DDL. Turn the front panel INPUT LEVEL control fully clockwise. Adjust the gain control (second from the left) so that the PEAK front panel LED is just turning on. Attach the distortion meter probe to pin 8 of the output (right hand) compander card. Adjust the HF distortion control on the left of the compander for minimum distortion. Reduce the input frequency to 80Hz and adjust the LF distortion for minimum distortion. As this adjustment may have some affect on level, repeat the first two steps of this procedure as required.

OUTPUT COMPANDER. With the input signal at 1KHz, adjust the front panel INPUT LEVEL control so that the left four level indicating LED's are illuminated. Alternating between 1KHz and 80Hz, adjust the HF and LF distortion controls for minimum distortion as measured at the output connector of the DDL. When distortion has been minimized, increase the INPUT LEVEL control until the PEAK LED just comes on. Now, adjust the output gain control on the compander card (second from the right) until the signal measured between pin 1 and pin 3 of the output connector measures about 20V peak to peak or about 6.5V rms.

As a final check, increase the signal level at the DDL input by 2dB. The output should begin to show clipping at this level.

PAUSE LEVEL CONTROL: Place the DDL in the PAUSE mode and monitor IC-55 pin 1 with the scope. Reduce the input signal to 40dB below clipping and adjust the control (R1) until the signal is just changing state. This adjustment may be made for different signal levels as detailed earlier.

A/B OFFSET CONTROL ADJUSTMENT (R3): This control is located to the left of IC-41 on the right rear of the circuit board. Its purpose is to equalize the DC levels of both output channels so that there is no DC shift when changing from the A output to the B output and back again. This control should be checked if any of the power supply regulators ever has to be replaced. Set the oscilloscope for a sweep rate of 5 milliseconds per division. Remove the input signal from the DDL and set the function control to the OSCillator position. Set the catchup rate fully counterclockwise. Attach the scope probe to pin 7 of IC-42. Depending upon the present setting of the control, you may observe a broken baseline with periodic level shifts. The fixed portion is about 30 milliseconds long, and the shifted portion is about 10 milliseconds. The relative polarities of these lines depend upon the control setting. The control should be adjusted to minimize the level shift. It is possible to adjust the control for zero shift, but it will drift slightly with age. Small shifts are generally below the noise level and may therefore be ignored, but if the control is seriously misadjusted, a "rumbling" quality can be imparted to the signal at high catchup rates.

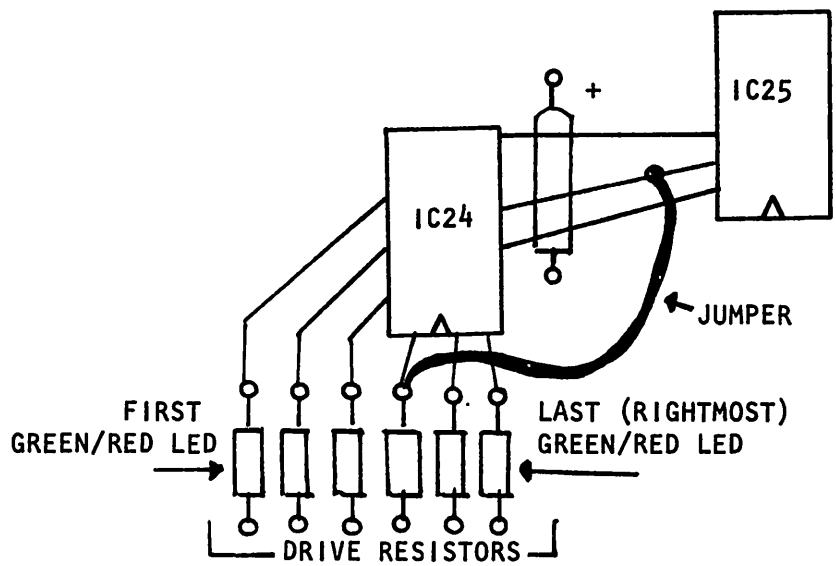
"FULL GATE" INPUT DIP SWITCH: This group of switches is adjusted at the factory, and together with the configuration ROM's, LC oscillator values, and filter components determines the configuration of the DDL in terms of frequency response and delay. This control should be set depending upon the number of delay cards installed in the unit (regardless of frequency response):

8 cards: 3,4,5, and 6 ON. (For units with s/n B95758 & Above, please
4 cards: 3,4, and 5 ON see note at the bottom of BD955 page 20.)
2 cards: 3 and 4 ON

The other switches have no function on the standard unit but may be used for custom modifications. If they are in use, this manual will contain an addendum covering their operation.

DUMP LAMP JUMPER: This is a short wire that is used to determine when, in relation to the total delay, the light in the DUMP switch becomes illuminated. By changing the jumper location, one may select different time intervals. See drawing below.

DUMP LAMP JUMPER LOCATION

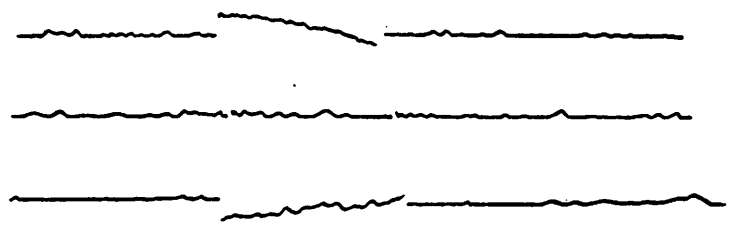


A/B OFFSET POT ADJUSTMENT

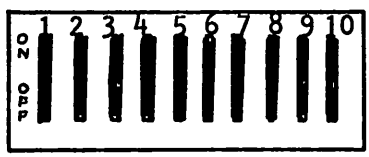
INCORRECT

CORRECT

INCORRECT



DIPSWITCH



TROUBLESHOOTING, emergency and otherwise:

The BD955 is a reasonably complicated electronic device, employing several hundred semiconductor devices, including the "state of the art" 16K Random Access Memory. It has been designed to achieve high reliability by using low power components, a conservatively rated power supply, and taking care to avoid potential problems. None of the foregoing means that it can't break down, however, and this section is designed to help you get it going again.

Despite the plethora of IC's in the unit, it is possible to check it systematically. The potential problems can be broken into three major areas: The first is a system problem that prevents it from working at all. This could be a power supply or audio chain defect, or some problem in the timing chain. The second (and we think most likely) is a RAM failure. Finally, some problem in the JUMP circuitry could manifest itself. Of the three, only the first is really serious. A RAM problem, as will be seen, can almost inevitably be repaired in the field in a few minutes. A JUMP circuit problem can be gotten around temporarily by using maximum manual delay and troubleshot at leisure. Here are some abbreviated procedures:

TIMING CHAIN: Check pin 7 of IC-50. If pulses of the proper width and frequency are present, it means that the timing dividers are almost certainly working properly. If they aren't, work backwards to the master oscillator to find the defect.
POWER SUPPLY: Check for +5, +15, and -15 volts on the thick lines near the rear of the circuit board. Check for +12 and -5 volts on the memory plug in boards. If -5 is missing, you have a bad chip or shorted bypass capacitor: remove boards to isolate the problem.
AUDIO CHAIN: Ordinary signal tracing procedures will work here. Just follow the signal through the unit and change anything that seems to be stopping it.

COMPANDERS: The two compander cards are identical. If a problem is found with one, they can both be bypassed (with, of course S/N degradation) and the unit put back in service until the replacement arrives.
RANDOM ACCESS MEMORY: A RAM problem will normally manifest itself with a periodic (once every 6.4, 3.2, or 1.6 second) click or burst of noise. The click usually indicates a bad single bit. The burst of noise can indicate a completely bad chip or bad card. The fastest way to locate the bad chip is as follows: Put in a tone and set the unit to the first delay step. As you listen to the output, monitor each row of RAM's successivly with a scope probe on the CAS line (pin 15 on each chip). Normally this pin is sitting at +5V. It will be pulsed low when the RAM is active. You have found the bad row when the pulse goes low coincident with the audible problem. Finding the defective chip may be done in two ways: The analytical method is to look at pin 7 of IC-42, the D/A converter. A most significant bit error (rightmost chip looking at the unit from the front) will give a 10Volt glitch or burst. Each chip to the left will cut the voltage in half. Another way is to simply substitute a different chip. Use the leftmost chip in any row for a temporary substitute.

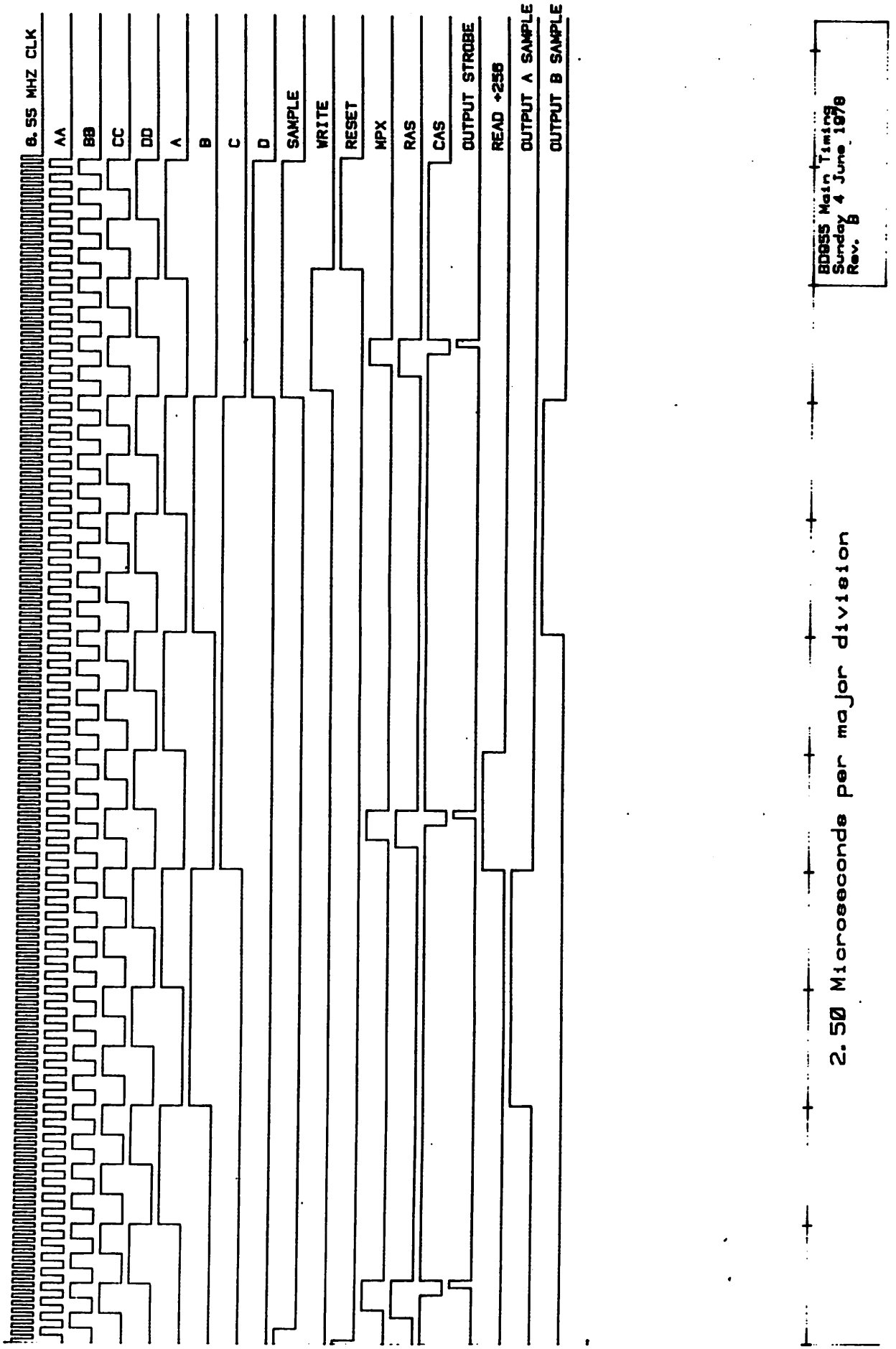
Return the defective chip to us for replacement. It is perfectly OK to run the unit with a missing RAM in the left hand column. The only audible effect will be a small (probably unnoticeable) increase in noise every 6.4, 3.2, or 1.6 seconds.

There is enough information in the Theory of Operation section and schematic diagrams to enable the technician to repair virtually any fault in the delay unit. Only an abbreviated summary, covering the most likely, most obvious, or most serious defects was given above. We are, of course, available for consultation on or repair of equipment, whether in or out of warranty, should this be necessary. If you do have to return the unit, be sure to read the portion of the warranty describing preferred shipping methods. Two large DON'T'S: DON'T ship loose circuit cards without wrapping them in conductive foil, and DON'T ship ANYTHING without a trouble report and return shipping instructions.

A few words about EVENTIDE

We are a small but dedicated organization which was founded in 1970. We have, until the advent of the BD955 broadcast delay line, manufactured equipment designed primarily for use in professional recording studios and by performing musicians. A recent (October 1977) survey by Billboard magazine shows us (under the heading "Delay Systems") as having our equipment in 44.9% of the studios surveyed. The next closest entry was 14.9%. Our most popular unit, the Eventide Harmonizer (TM) has found use in many broadcast stations as a production tool: it is capable of simultaneous delay and true pitch change. We would be happy to provide further information on this or any of our other products, if you will indicate your desires on the warranty card.

If you have any questions, problems, concerns, or simply want to discuss any aspect of our equipment (including special requirements or modifications), we suggest that you call after 6PM New York time, for the following reasons: It's cheaper, and its usually possible to give you unrushed and undivided attention. We are not a company of clock watchers, but we are extraordinarily busy! Of course, we are happy to talk to you during the day, but we won't be quite as sociable.


8.55 MHZ CLK
AA
BB
CC
DD
A
B
C
D
SAMPLE
WRITE
RESET
MPX
RAS
CAS
OUTPUT STROBE
READ +256
OUTPUT A SAMPLE
OUTPUT B SAMPLE
BD855 Main Timing
Sunday 4 June 1978
Rev. B
2.50 Microseconds per major division

Eventide
the next step

To all users of BD955 Broadcast Delay Lines (WITH SERIAL NUMBER B95757 AND BELOW ONLY)

(originally mailed August 1980)

We have recently been hearing from some stations who bought BD955 Delay Lines with either 1.6 or 3.2 seconds of delay, and are now finding that their insurance coverage against libel suits is not valid unless they are providing six seconds of delay protection on their telephone talk shows. Check with your legal department to see if this is true in your case.

It is possible to increase the maximum delay of your BD955 very simply, by adding the required number of memory cards (see below), and by changing two socketted integrated circuits.

IT IS NOT PRACTICAL TO CHANGE THE FREQUENCY RESPONSE OF THE UNIT.

Delivery of memory cards and the necessary IC's is from stock. Each card costs $600, and the set of IC's and card sockets costs $25 per unit, plus shipping. The change is well documented, and may easily be done in the field by a competent maintenance engineer. If you would prefer us to adapt your unit, there will be an additional charge of $55 per unit for labor, plus shipping. Turnaround time from receipt to return shipping is typically 48 hours.

BD955 Broadcast Delay Lines can also be retrofitted for stereo operation (one unit configured as a master, one as a slave). The charge for this is $27.50 for labor, plus $150 for the stereo option, and shipping.

NUMBER OF MEMORY CARDS NEEDED TO BRING UNITS UP TO 6.4 SECONDS MAXIMUM DELAY

If your unit's configuration is currently:		you will need this many cards to bring it up to 6.4 seconds:
15 kHz	1.6 seconds	6
15 kHz	3.2 seconds	4
7.5 kHz	1.6 seconds	3
7.5 kHz	3.2 seconds	2

plus the set of IC's and sockets

Please remember to reference the serial number of your unit in any communication.

Eventide
the next step

INSTRUCTIONS FOR INCREASING THE MAXIMUM DELAY OF A BD955 BROADCAST DELAY LINE (WITH SERIAL NUMBER B95757 AND BELOW ONLY)

1. You will receive the following items:

   a) B951 memory cards (number varies according to existing delay and delay required).
   b) Card sockets - these may already be installed in your unit.
   c) Card supports.
   d) Two PROM's, marked 24 and 63. NOTE: These are not interchangeable.

2. Remove top cover of BD955. If your unit is already fitted with sufficient card sockets, proceed to step 6 below.

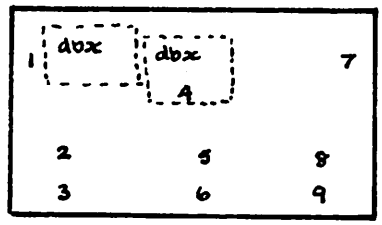
3. Remove bottom cover (there are nine screws, one of which is under the dbx card. See diagram).

4. Solder in card sockets (make sure these are flush to the board before soldering).

5. Replace bottom cover.

6. Insert card supports.

7. Insert cards.

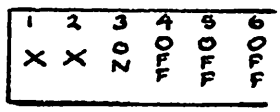


location of screws holding bottom cover

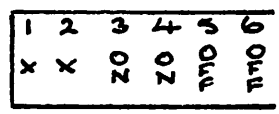
8. Replace IC's 24 and 63 with new IC's. DO NOT CONFUSE OLD AND NEW.

9. Change the settings of the DIP switch as shown, to match the number of cards now in your unit.

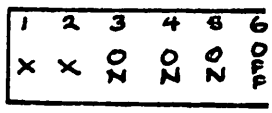
one card



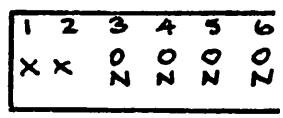
two cards



four cards

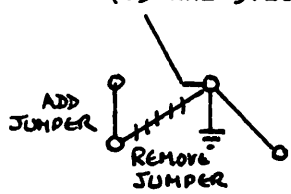


eight cards

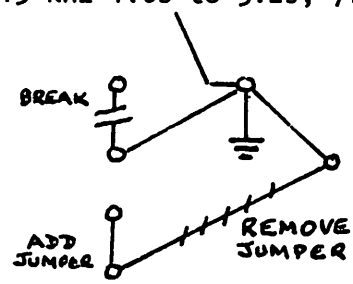


10. Locate the GROUND (EARTH) symbol in the center of the main board. Make changes as shown:

4-card to 8-card
(15 kHz 3.2s to 6.4s)



2-card to 4-card
(15 kHz 1.6s to 3.2s, 7.5 kHz 3.2s to 6.4s)



Eventide
the next step

INSTRUCTIONS FOR INCREASING THE MAXIMUM DELAY OF A BD955 BROADCAST DELAY LINE (WITH SERIAL NUMBER B95758 AND ABOVE ONLY) FROM 3.2 TO 6.4 SECONDS.

1. You will need the following items:

   a) 20 pieces 64K RAMs.
   b) 20 pieces IC sockets for 64K RAMs if not already on circuit board.
   c) 2 PROMS marked for IC24 and IC63.

2. Remove top cover.

3. Remove bottom cover only if sockets for 64K RAM are not present.

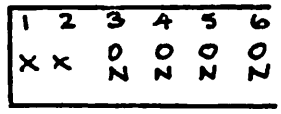
4. If sockets are not present, solder them flush to mother board noting proper orientation.

5. Replace bottom cover if necessary.

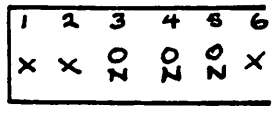
6. Insert 64K RAM memory chips, noting proper orientation.

7. Replace IC24 and IC63 with new IC's. Do not confuse old with new.

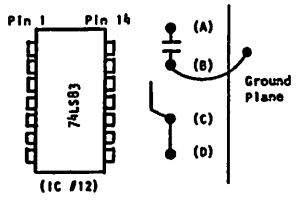
8. a. For units with 15kHz bandwidth, dip switches on switch 1 (sw1, see page A-1a/A-1b) should be set as follows:

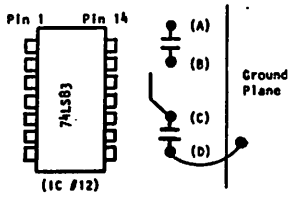


   b. For units with 7.5kHz bandwidth, set sw1 as follows:



9. Locate the ground plane in the center of the main board. Depending upon the frequency response of the unit, make the following changes:



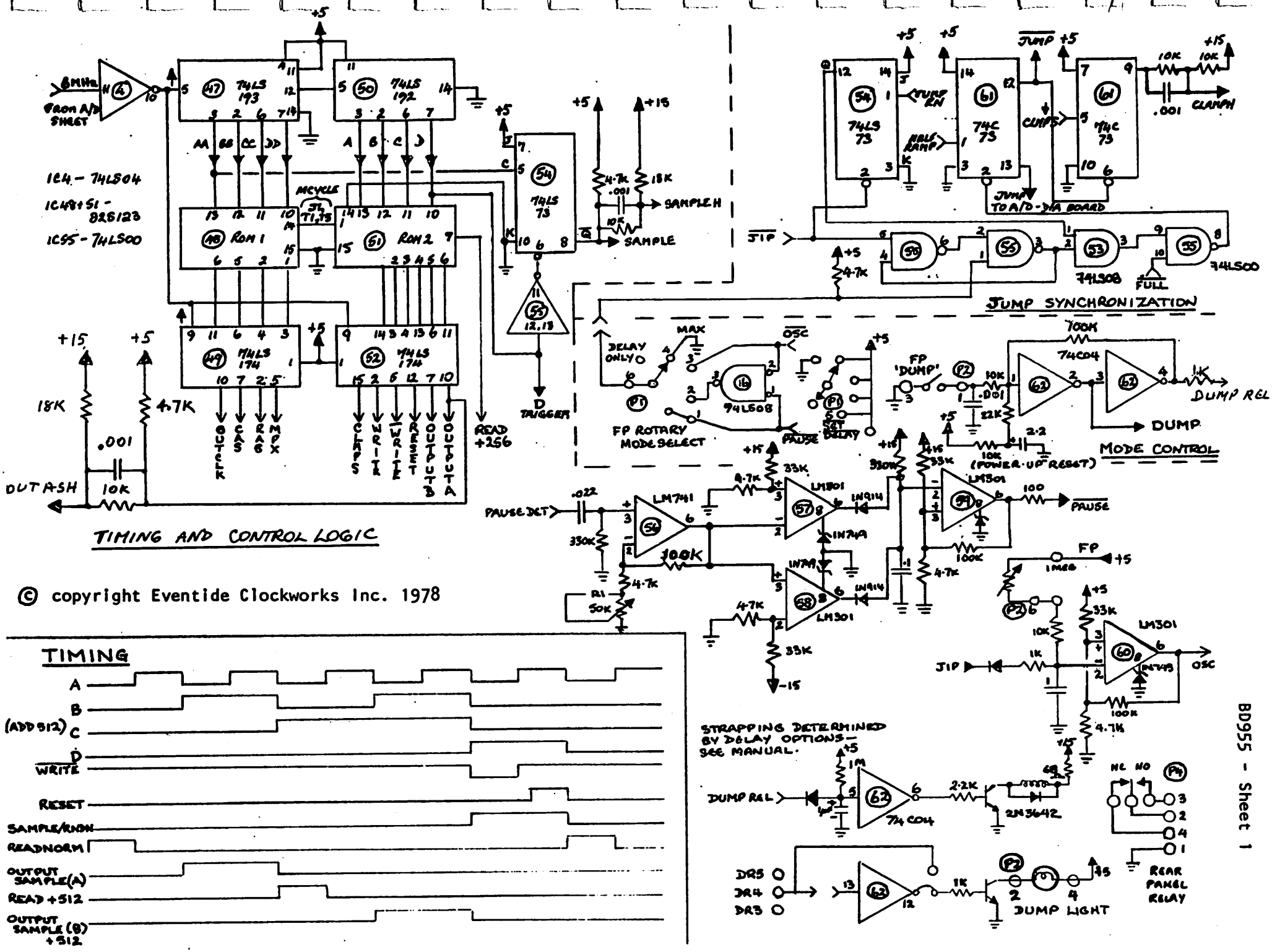


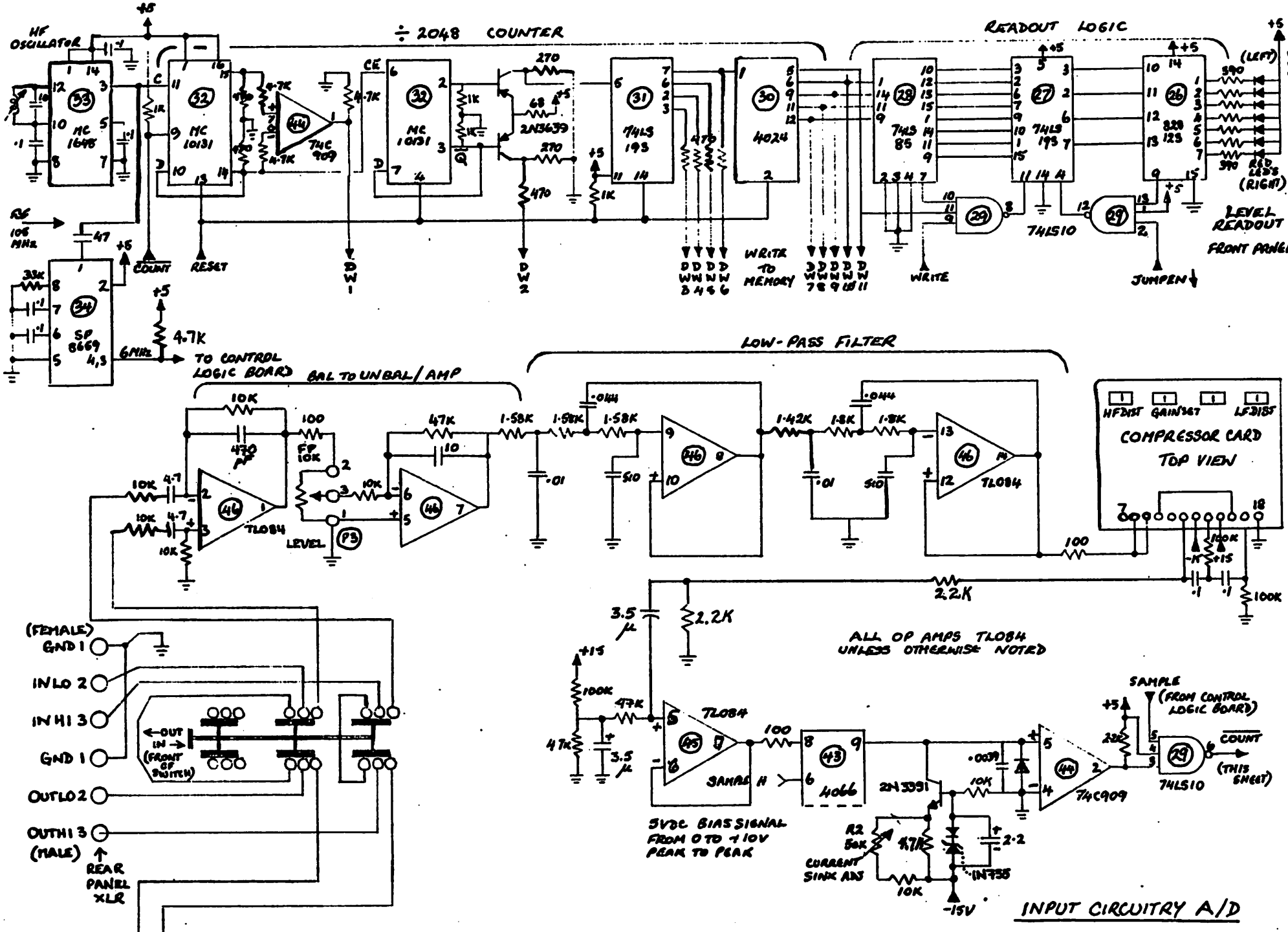
For units with 15kHz bandwidth:

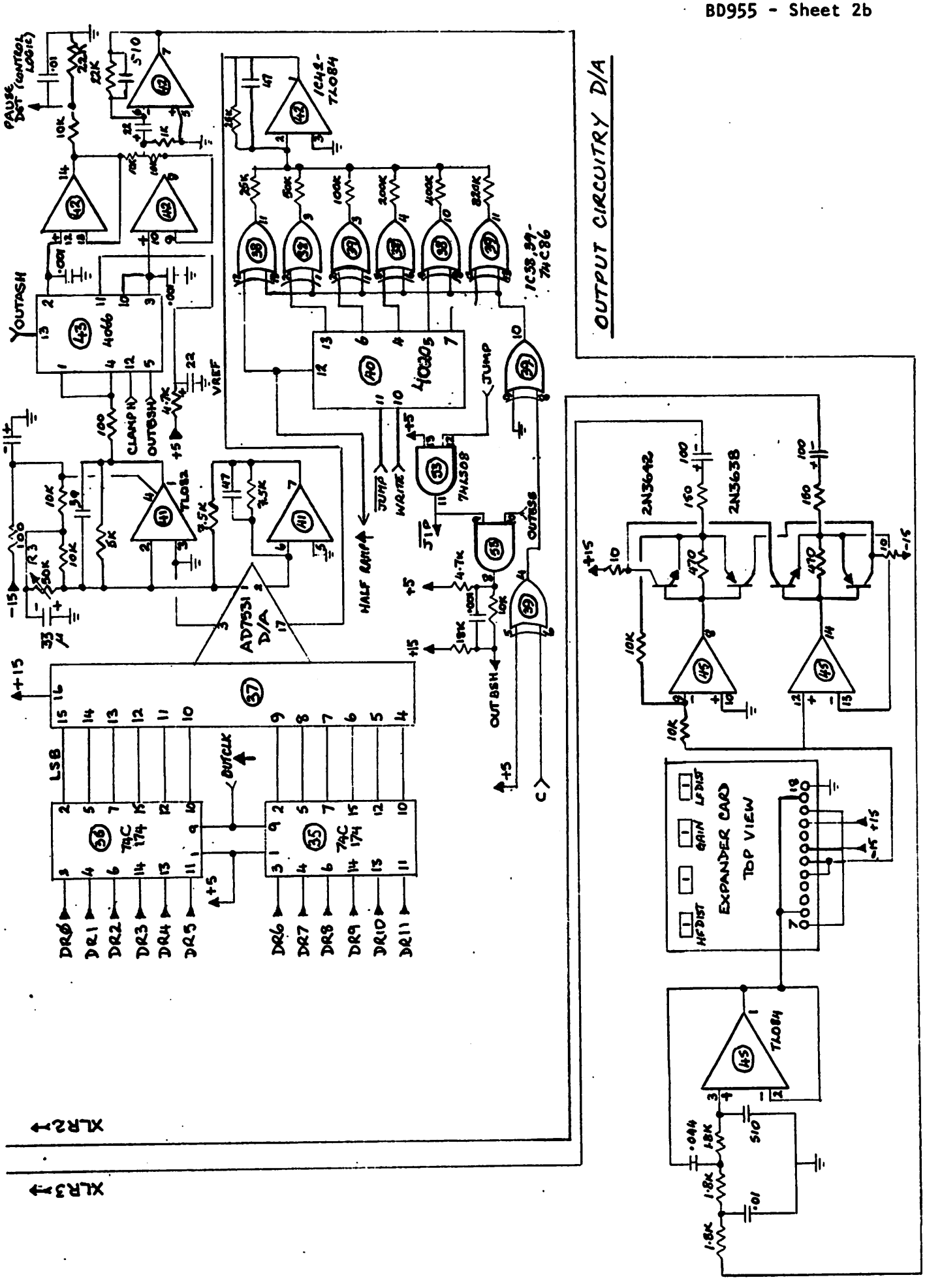
Remove jumper between (B) and ground plane and add jumper between (A) and (B).

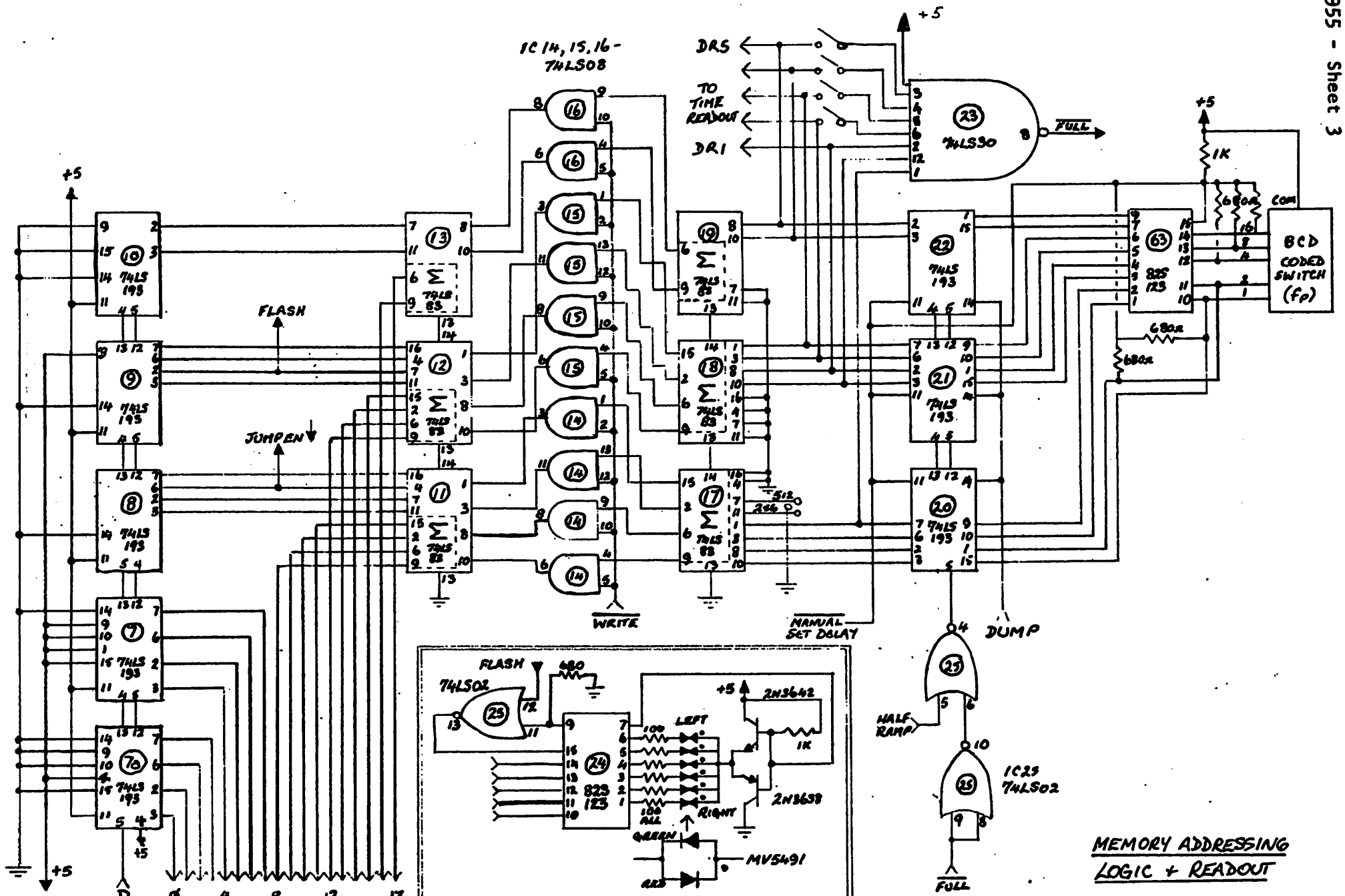
For units with 7.5kHz bandwidth:

Remove jumper between (D) and ground plane and add jumper between (C) and (D).









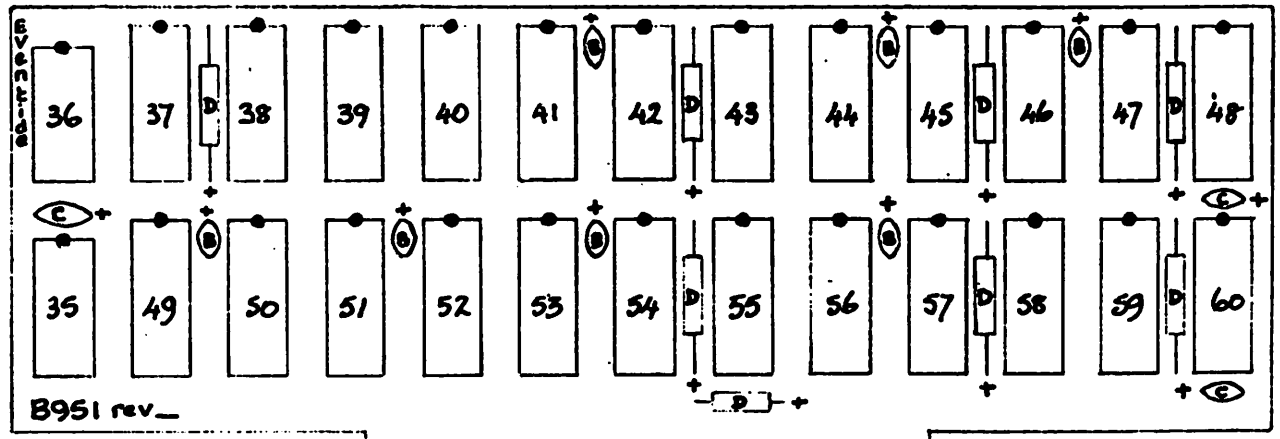
MEMORY BOARD PHYSICAL LAYOUT

TOP VIEW

(B) V_{BB} BYPASS CAPACITOR

(C) V_{CC} BYPASS CAPACITOR

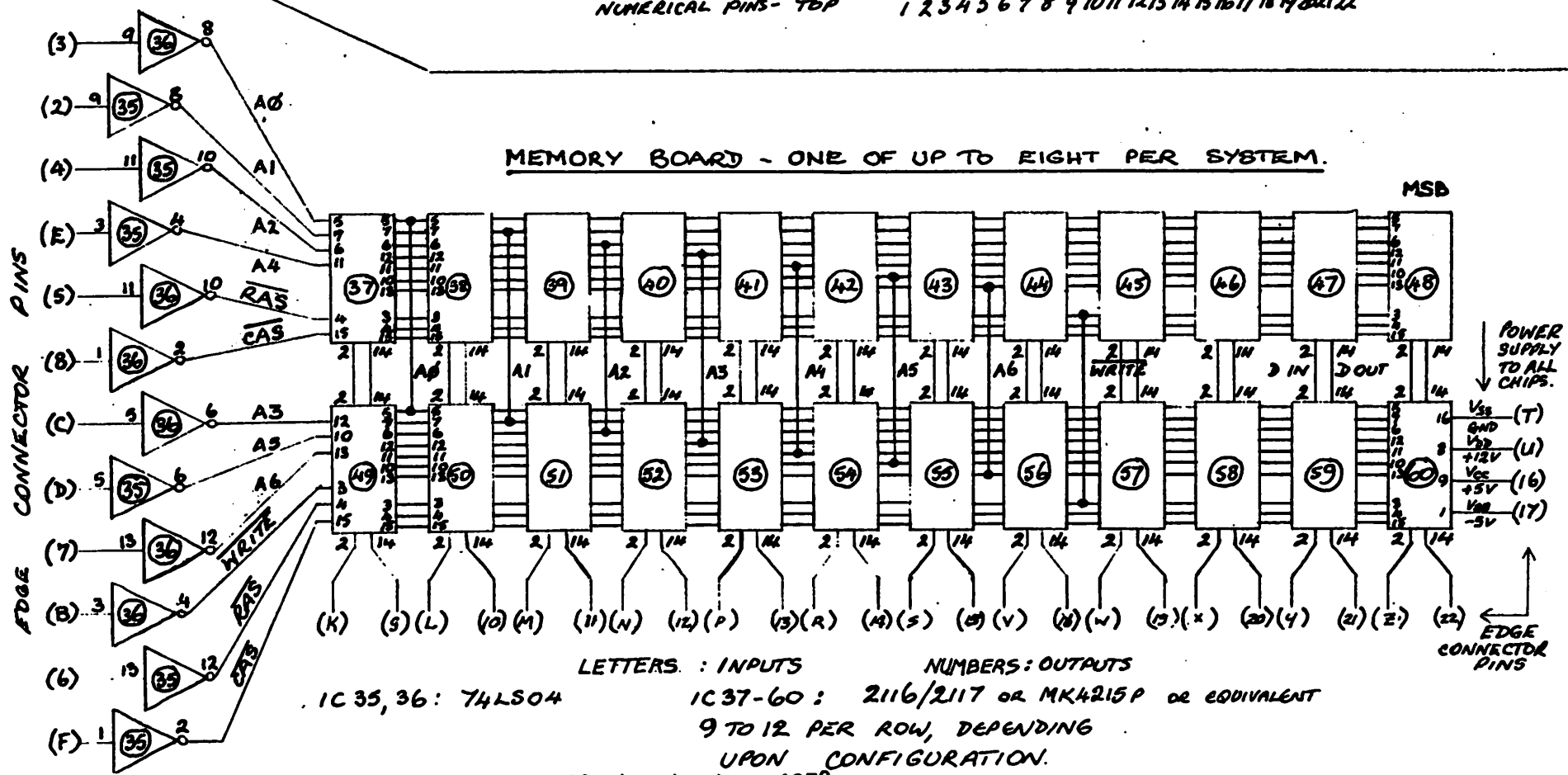
(D) V_{DD} BYPASS CAPACITOR



LETTER PINS - BOTTOM A B C D E F H J K L M N P R S T U V W X Y Z

NUMERICAL PINS - TOP 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22

MEMORY BOARD - ONE OF UP TO EIGHT PER SYSTEM.



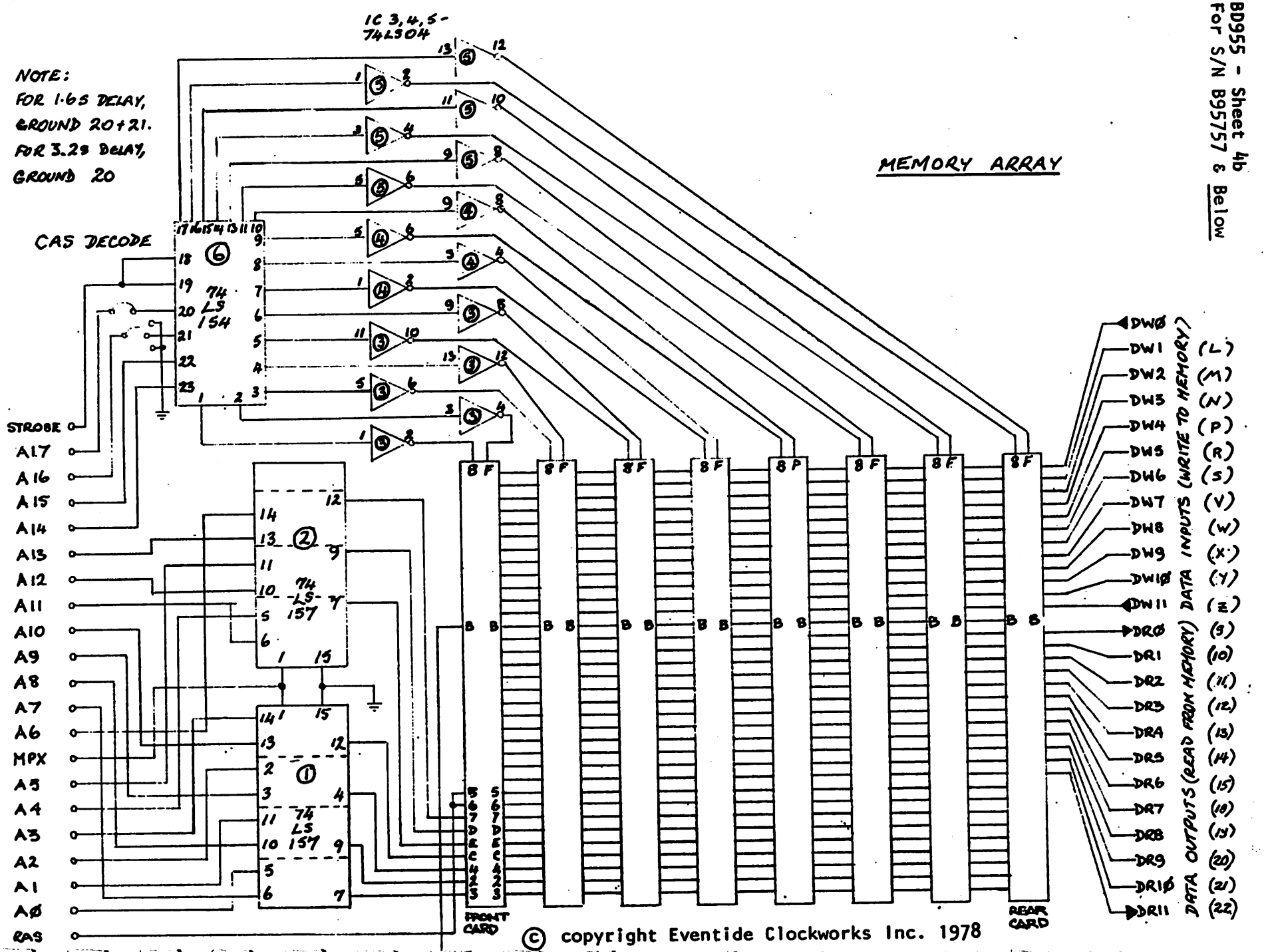
LETTERS : INPUTS NUMBERS : OUTPUTS

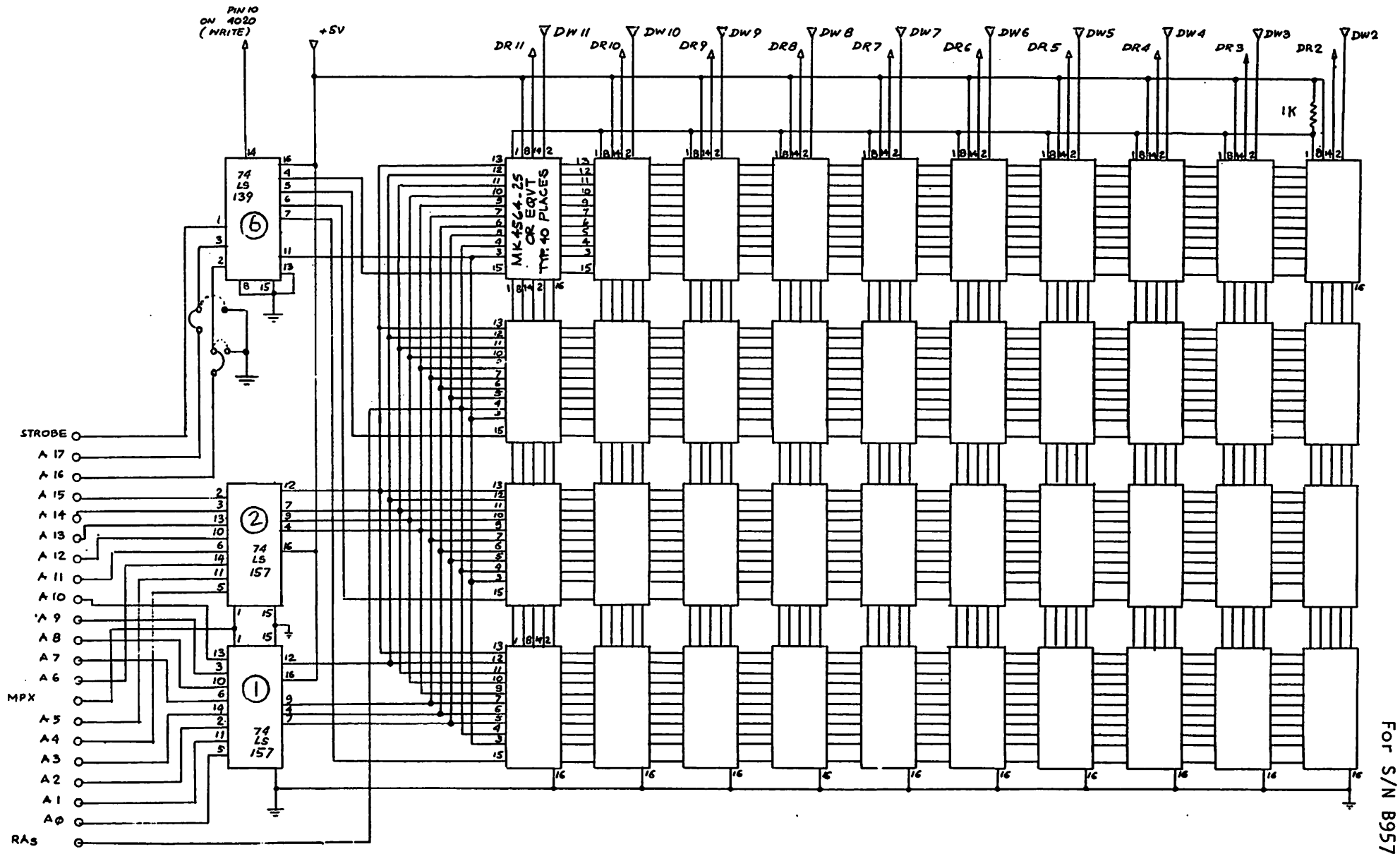
IC 35, 36 : 74LS04

IC 37-60 : 2116/2117 OR MK4215P OR EQUIVALENT

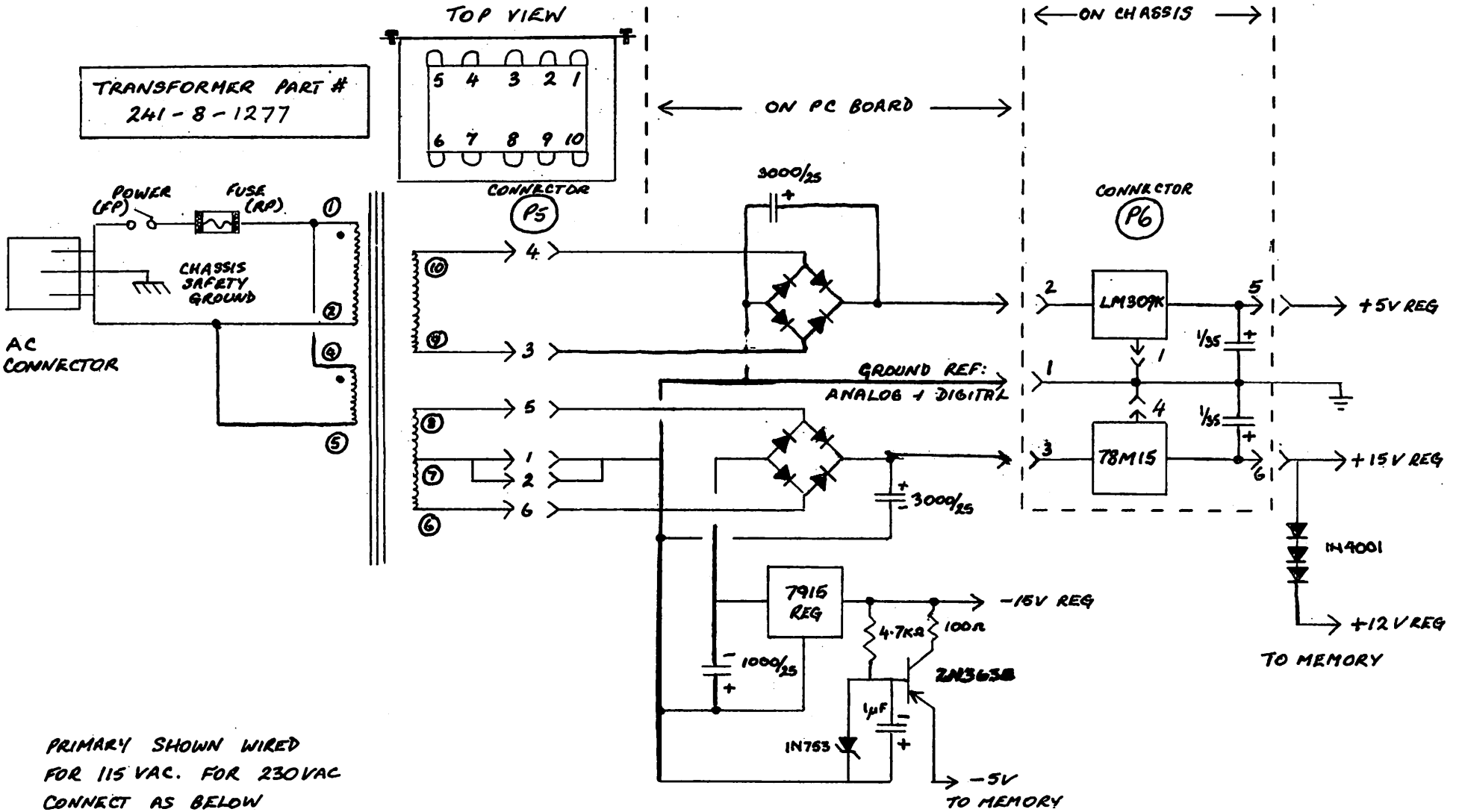
9 TO 12 PER ROW, DEPENDING UPON CONFIGURATION.

BD955 - Sheet 4a
For S/N B9575 & Below

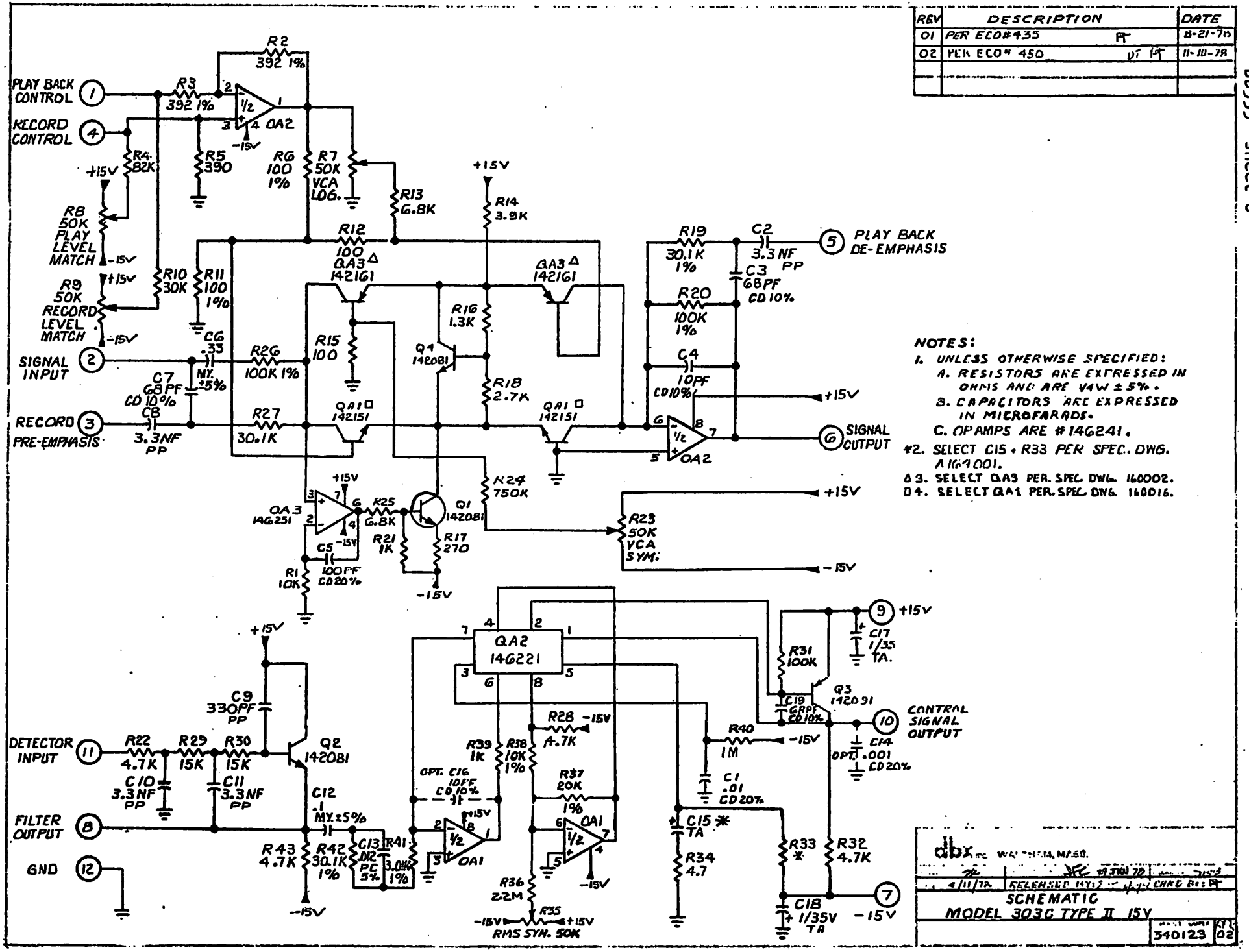




BD955 - Sheet 4c
For S/N B95758 & Above

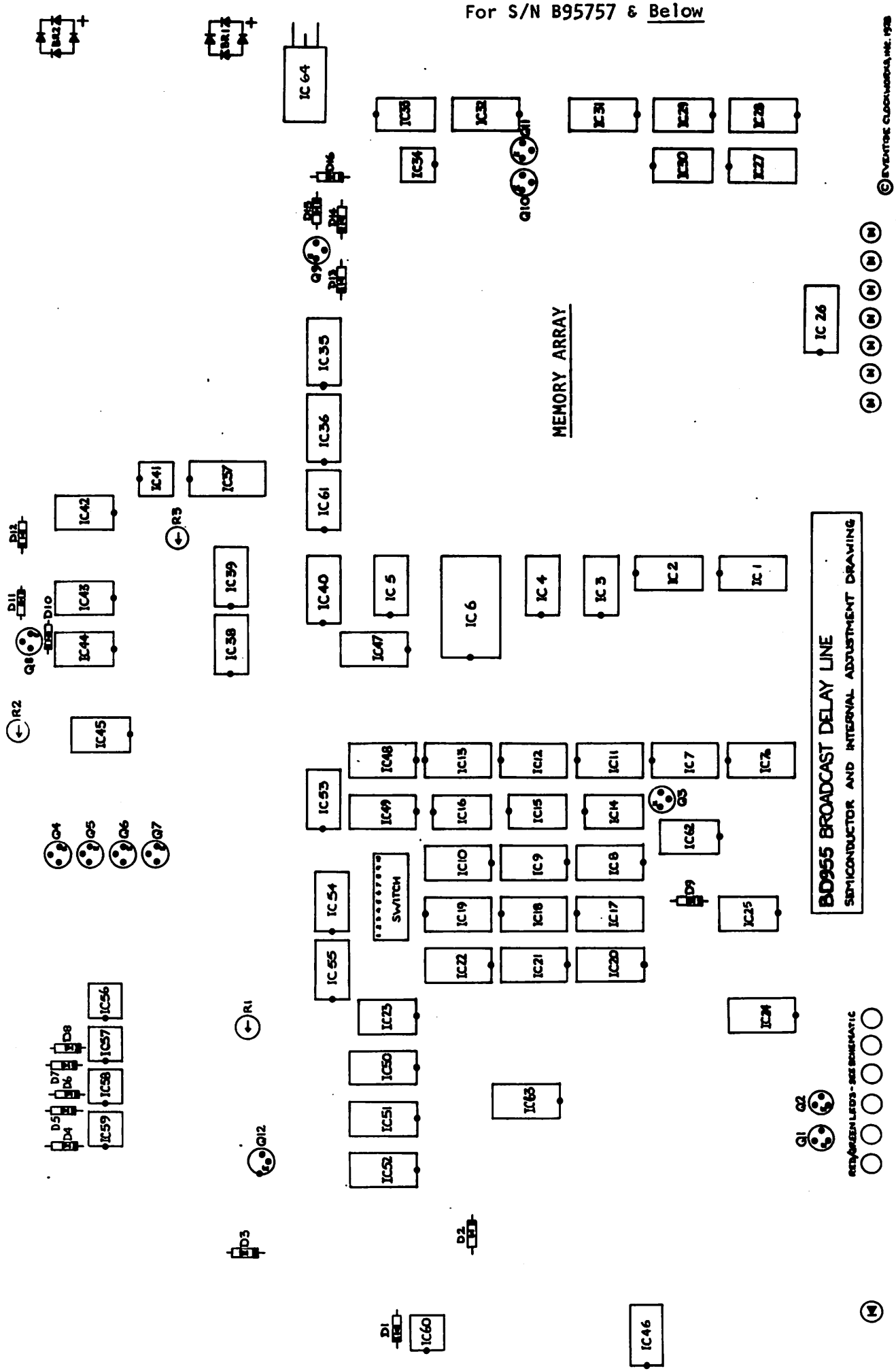


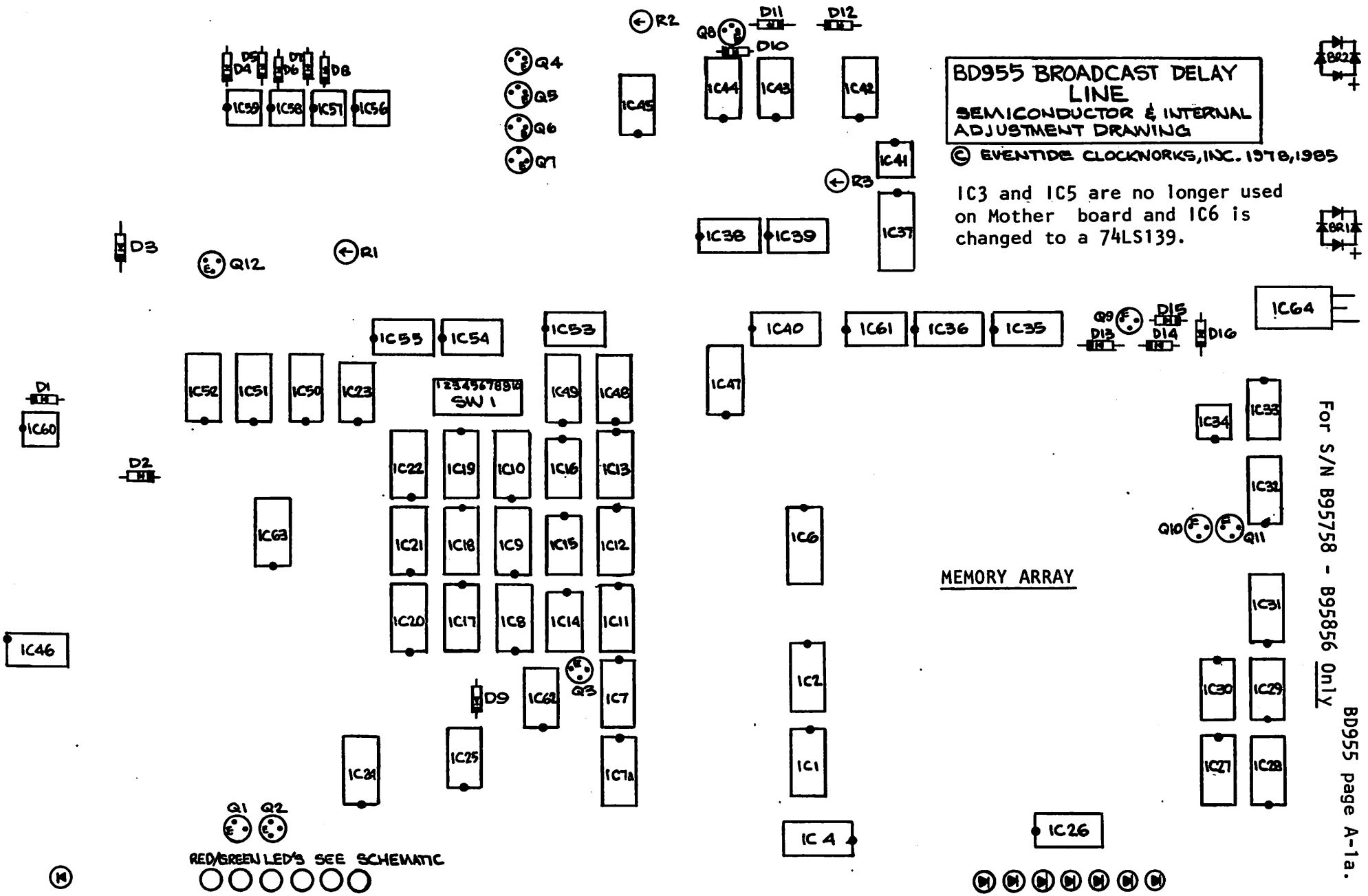
BD955 POWER SUPPLY/CHASSIS

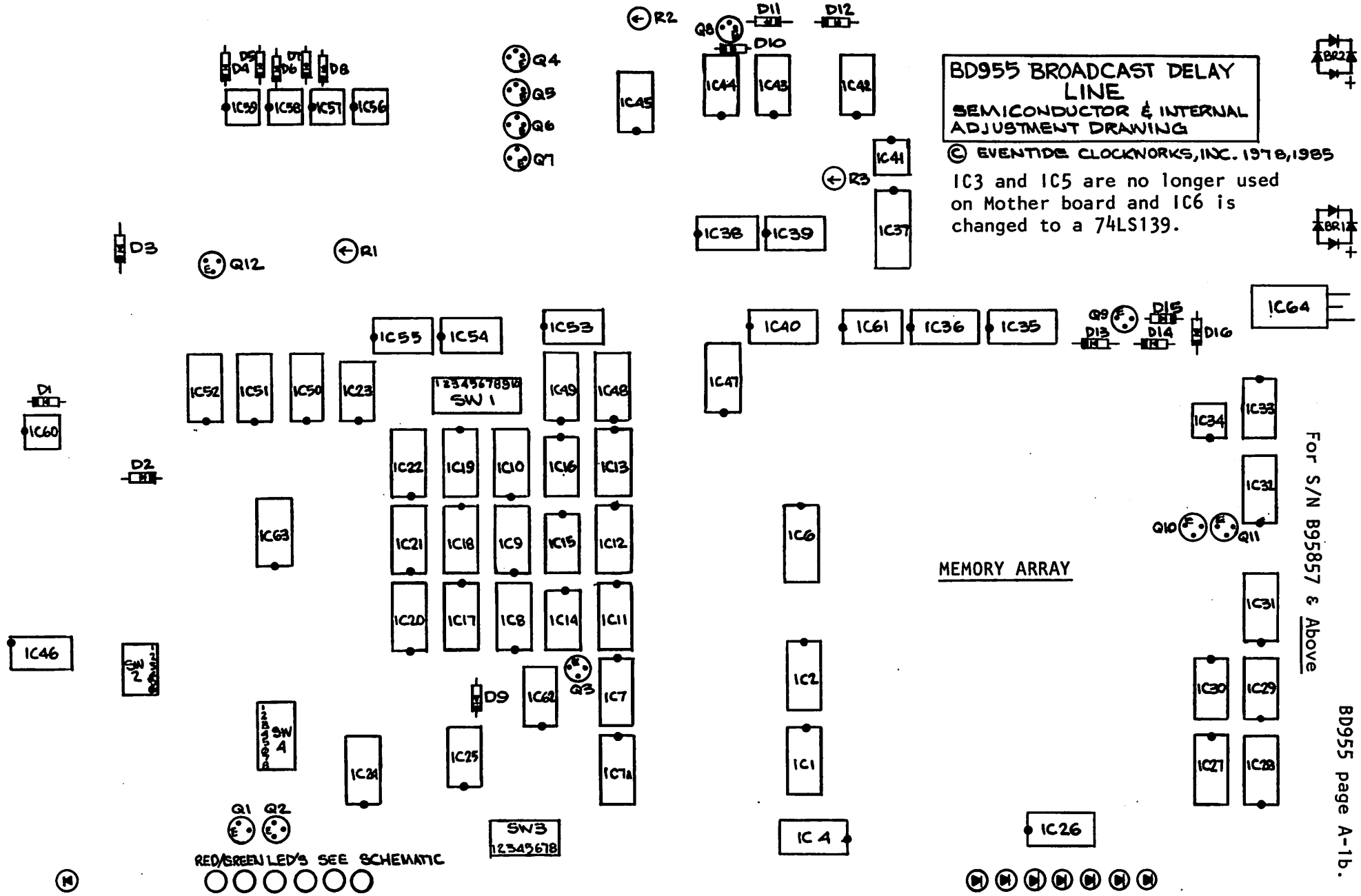


BD955 sheet 6

For S/N B95757 & Below




BD955 BROADCAST DELAY LINE
SEMICONDUCTOR & INTERNAL ADJUSTMENT DRAWING
© EVENTIDE CLOCKWORKS, INC. 1978, 1985
IC3 and IC5 are no longer used on Mother board and IC6 is changed to a 74LS139.
MEMORY ARRAY
RED/GREEN LED'S SEE SCHEMATIC
SW 1
For S/N B95758 - B95856 Only
BD955 page A-1a.


BD955 BROADCAST DELAY LINE
SEMICONDUCTOR & INTERNAL ADJUSTMENT DRAWING
© EVENTIDE CLOCKWORKS, INC. 1978, 1985
IC3 and IC5 are no longer used on Mother board and IC6 is changed to a 74LS139.
MEMORY ARRAY
RED/GREEN LED'S SEE SCHEMATIC
For S/N B95857 & Above
BD955 page A-1b.

APPENDIX Diodes and Transistors used in the BD955 Broadcast Delay Line

DIODE #	PART.	DIODE #	PART	DIODE #	PART
1	1N749	7	1N749	13	1N4001
2	1N914	8	1N914	14	1N4001
3	1N914	9	1N914	15	1N753
4	1N749	10	1N914	16	1N4001
5	1N749	11	1N914		
6	1N914	12	1N755		

RED LED's - NATIONAL NSL 5053

RED/GREEN LED's - MONSANTO MV5491 OR OPCOA LST710L

TRANSISTOR #	PART	TRANSISTOR #	PART
1	PN3642	8	PN3391
2	PN3638	9	PN3638
3	PN3642	10	2N3639
4	PN3642	11	2N3639
5	PN3838	12	PN3642
6	PN3638		
7	PN3642		

APPENDIX Integrated Circuits used in the BD955 Broadcast Delay Line

IC#	PART	IC#	PART	IC#	PART
1	74LS157	26	82S123	52	74LS174
2	74LS157	27	74LS193	53	74LS08
**3	74LS04	28	74LS85	54	74LS73
4	74LS04	29	74LS10	55	74LS00
**5	74LS04	30	CD4024	56	LM741
**6	74LS154	31	74LS193	57	LM301A
7	74LS193	32	MC10131	58	LM301A
7A	74LS193	33	MC1648	59	LM301A
8	74LS193	34	SP8659A	60	LM301A
9	74LS193	35	74LS174	61	74C73
10	74LS193	36	74LS174	62	74C04
11	74LS83	37	AD7531	63	82S123
12	74LS83	38	74C86	64	7915
13	74LS83	39	74C86		
14	74LS08	40	CD4020		
15	74LS08	41	TL082		
16	74LS08	42	TL084		
17	74LS83	43	CD4066		
18	74LS83	44	74C909		
19	74LS83	45	TL084		
20	74LS193	46	TL084		
21	74LS193	47	74LS193		
22	74LS193	48	82S123		
23	74LS30	49	74LS174		
24	82S123	50	74LS192		
25	74LS02	51	82S123		

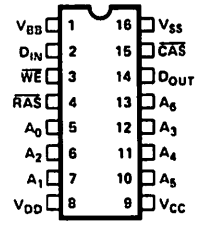
**PLEASE NOTE: FOR S/N B95758 and ABOVE, IC3 and IC5 are no longer used on Mother Board and IC6 is changed to a 74LS139.

APPENDIX Integrated Circuits used in the BD955 Broadcast Delay Line

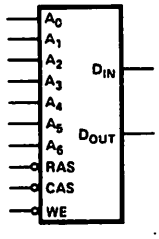
Part number	Description	IC number
various	16K Dynamic Random Access Memory (memory card)	39-48 & 51-60
74C04	Hex Inverter	62
74C73	Dual J-K Flip-Flop with Clear	61
74C86	Quad 2-Input EXCLUSIVE-OR Gate	38,39
74C909	Quad Comparator	44
CD4020	14-stage Ripple-Carry Binary Counter/Divider	40
CD4024	7-stage Ripple-Carry Binary Counter/Divider	30
CD4066	Quad Bilateral Switch	43
LM301A	Operational Amplifier	57-60
LM741	Operational Amplifier	56
TL082	JFET-Input Dual Operational Amplifier	41
TL084	JFET-Input Quad Operational Amplifier	42,45,46
74LS00	Quad 2-Input NAND Gate	55
74LS02	Quad 2-Input NOR Gate	25
74LS04	Hex Inverter (memory card 35 & 36)	3,4,5
74LS08	Quad 2-Input AND Gate	14,15,16,53
74LS10	Triple 3-Input NAND Gate	29
74LS30	8-Input NAND Gate	23
74LS73	Dual J-K Negative Edge-Triggered Flip-Flop	54
74LS83A	4-Bit Binary Full Adder - Fast Carry	11-13, 17-19
74LS85	4-Bit Magnitude Comparator	28
74LS154	4-to-16 Decoder/Demultiplexer	6
74LS157	Quad 2-to-1 Multiplexer	1,2
74LS174	Hex D-Type Flip-Flop with Clear	35,36,49,52
74LS192	BCD Decade Up/Down Counter	50
74LS193	4-Bit Binary Up/Down Counter	7,7a,8,9,10,20,21,22,27,31,47
MC1648	Emitter-Coupled Voltage-Controlled Oscillator	33
MC10131	Dual D-Type Master/Slave Flip-Flop	32
AD7531	4-Quadrant Multiplying D/A Converter	37
82S123	256-Bit Bipolar PROM (32 x 8)	24,26,48,51,63
SP8659A	High Speed Divide by 16 Divider	34
LM309	5-Volt Regulator	chassis
7815UC	15-Volt Regulator	chassis
7915UC	Minus 15-Volt Regulator	64

Intel 2117-5 (or equivalent) - 16K Dynamic Random Access Memory

PIN CONFIGURATION



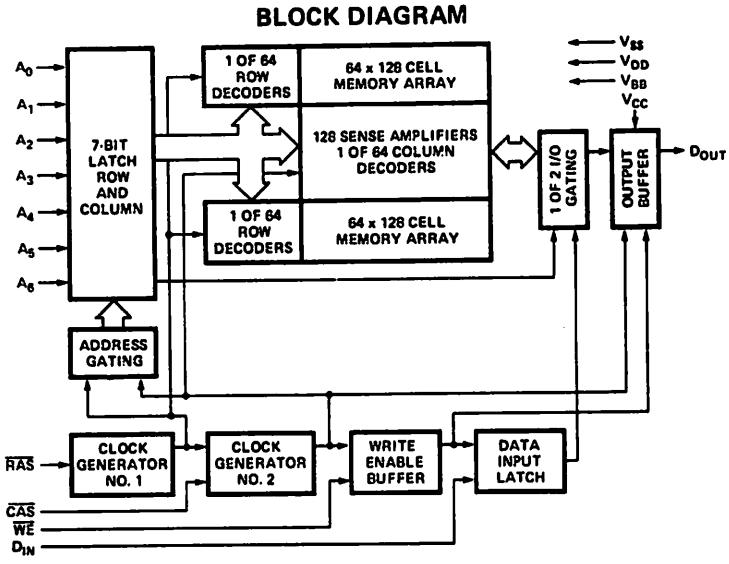
LOGIC SYMBOL



PIN NAMES

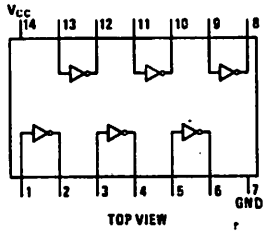
A_0-A_6	ADDRESS INPUTS	$\overline{WE}$	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
D_{IN}	DATA IN	V_{CC}	POWER (+5V)
D_{OUT}	DATA OUT	V_{DD}	POWER (+12V)
$\overline{RAS}$	ROW ADDRESS STROBE	V_{SS}	GROUND

BLOCK DIAGRAM

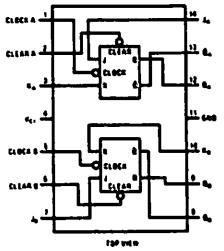


APPENDIX Integrated Circuits used in the BD955 Broadcast Delay Line

74C04 - Hex Inverter (also 74LS04)

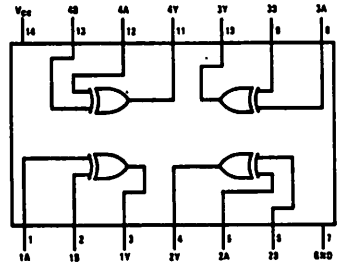


74C73 - Dual J-K Flip-Flop with Clear (also 74LS73)

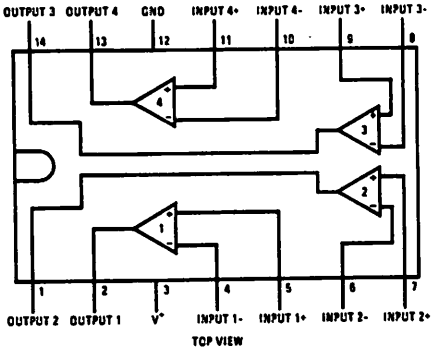


Note: A logic "0" on clear sets Q to logic "0."

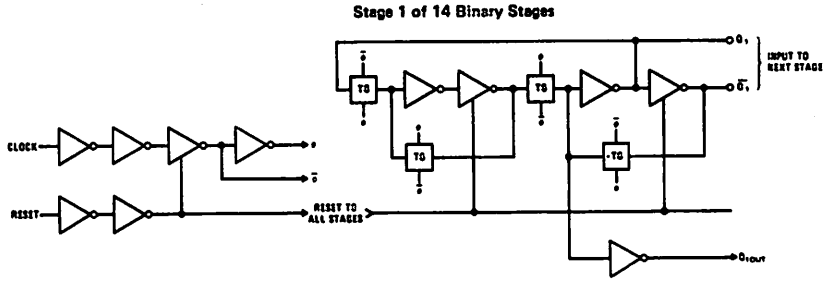
74C86 - Quad 2-Input EXCLUSIVE-OR Gate



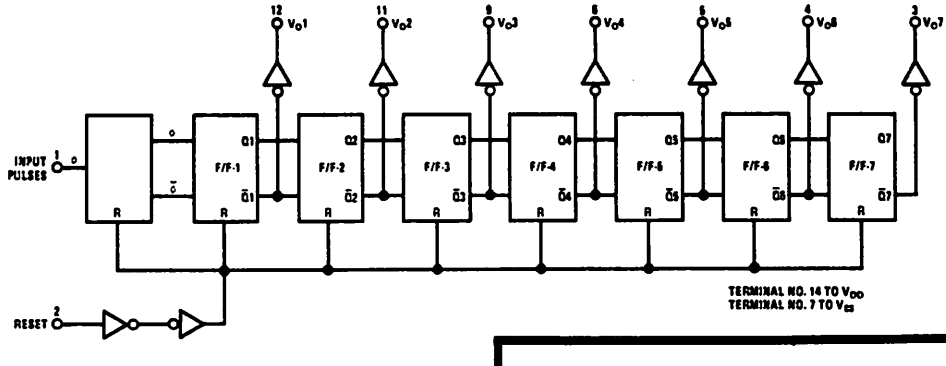
74C909 - Quad Comparator

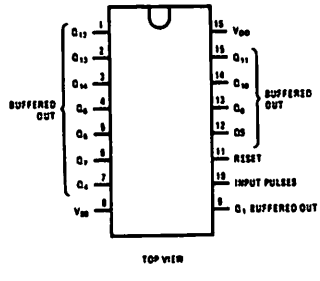


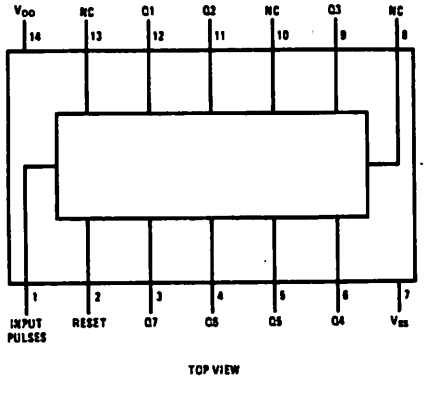
CD4020 - 14-stage Ripple-Carry Binary Counter/Divider



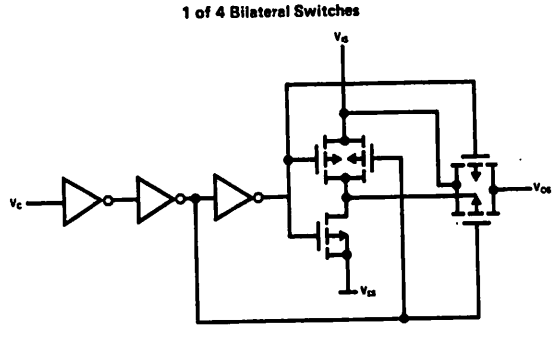
CD4024 - 7-stage Ripple-Carry Binary Counter/Divider

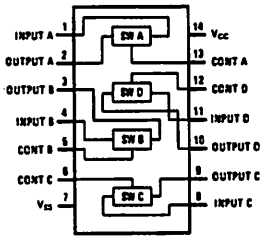






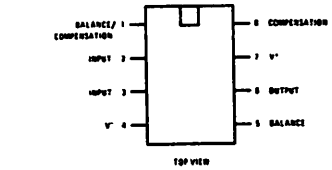
CD4066 - Quad Bilateral Switch

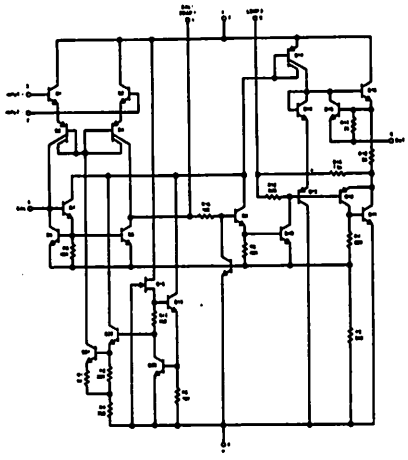




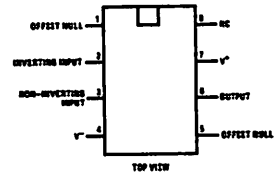
APPENDIX Integrated Circuits used in BD955 Broadcast Delay Line

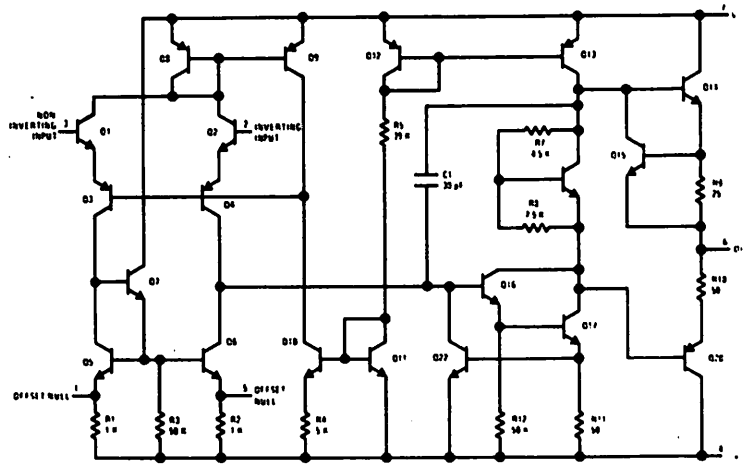
LM301A - Operational Amplifier



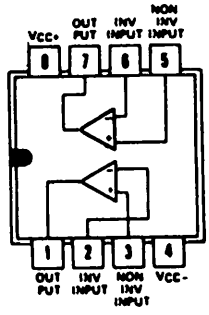


LM741 - Operational Amplifier

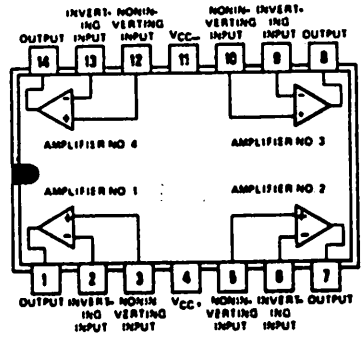




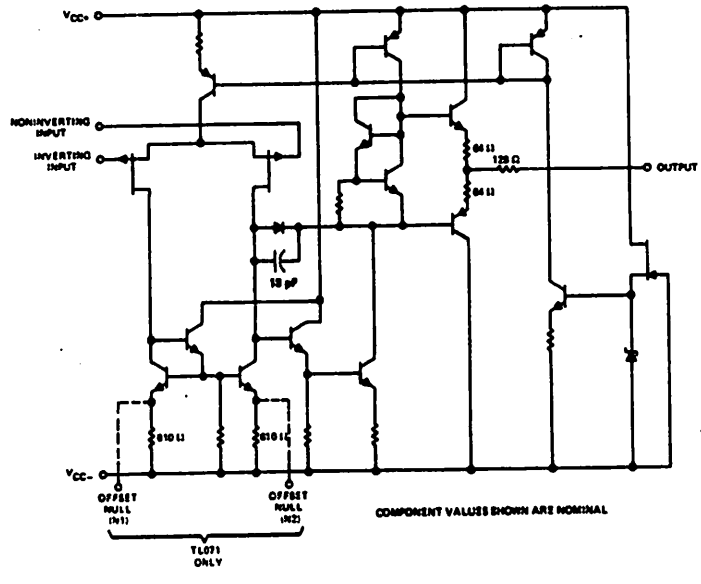
TL082 - JFET-Input Dual Operational Amplifier



TL084 - JFET-Input Quad Operational Amplifier

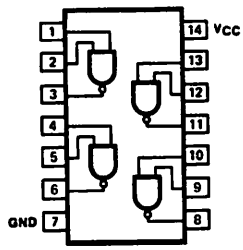


schematic (each amplifier)

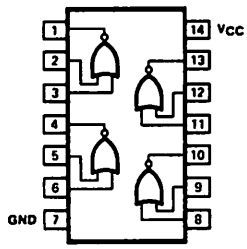


APPENDIX Integrated Circuits used in BD955 Broadcast Delay Line

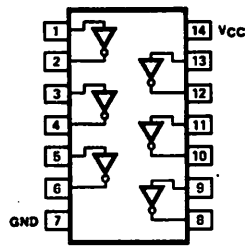
74LS00 - Quad 2-Input NAND Gate



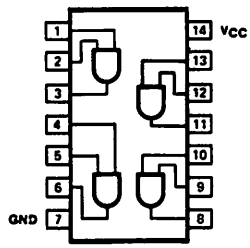
74LS02 - Quad 2-Input NOR Gate



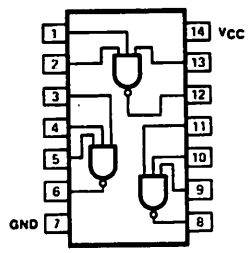
74LS04 - Hex Inverter (also 74C04)



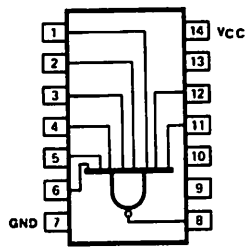
74LS08 - Quad 2-Input AND Gate



74LS10 - Triple 3-Input NAND Gate

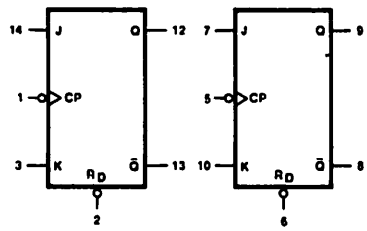


74LS30 - 8-Input NAND Gate



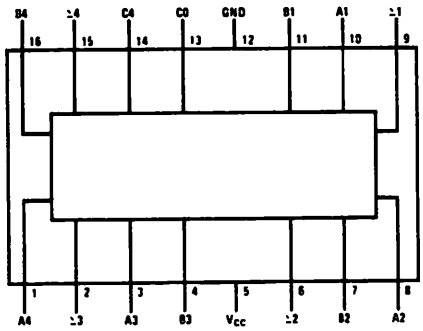
OC = Open Collector B = Buffer

74LS73 - Dual JK Negative Edge-Triggered Flip-Flop (see 74C73)

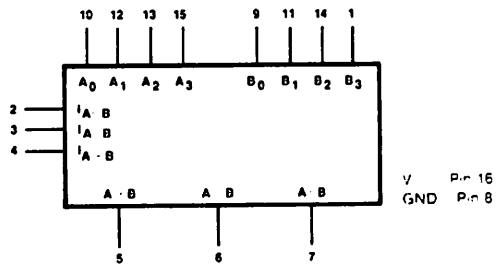


Vcc Pin 4
GND Pin 11

74LS83A - 4-Bit Binary Full Adder - Fast Carry

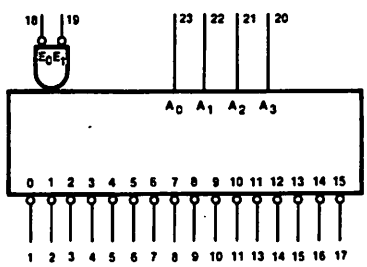


74LS85 - 4-Bit Magnitude Comparator



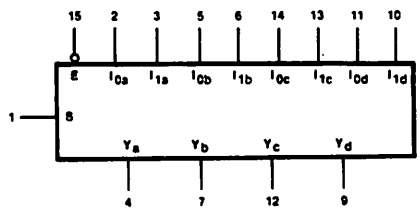
Vcc Pin 16
GND Pin 8

74LS154 - 4-to-16 Decoder/Demultiplexer



VCC = Pin 24
GND = Pin 12

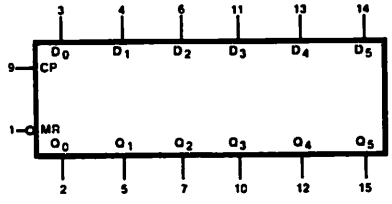
74LS157 - Quad 2-to-1 Multiplexer



VCC = Pin 16
GND = Pin 8

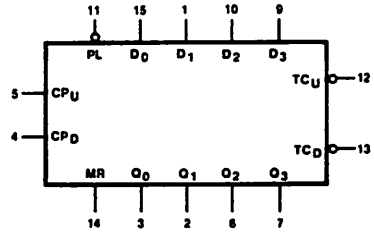
APPENDIX Integrated Circuits used in the BD955 Broadcast Delay Line

74LS174 - Hex D-Type Flip-Flop with Clear



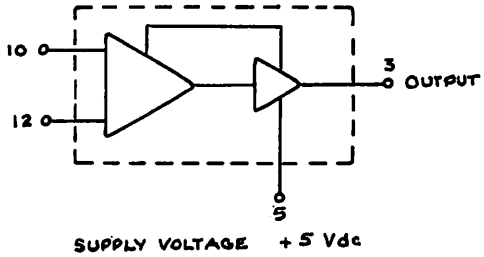
V_{CC} = Pin 16
GND = Pin 8

74LS192 - BCD Decade Up/Down Counter
74LS193 - 4-bit Binary Up/Down Counter



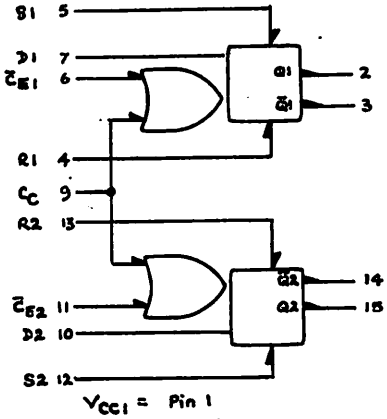
V_{CC} = Pin 16
GND = Pin 8

MC1648 - Emitter-Coupled Voltage-Controlled Oscillator



SUPPLY VOLTAGE	+5 Vdc
GROUND PINS	7, 8
SUPPLY PINS	1, 14

MC10131 Dual D-Type Master/Slave Flip-Flop



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

R-S TRUTH TABLE

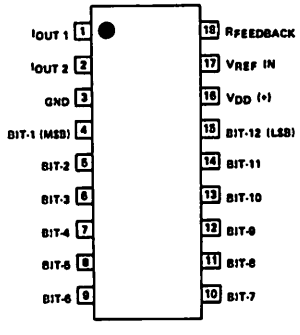
R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

CLOCKED TRUTH TABLE

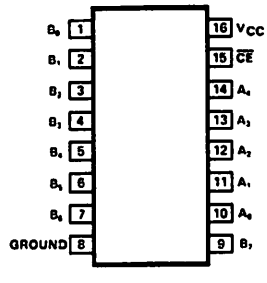
C	D	Q_{n+1}
L	ϕ	Q_n
H	L	L
H	H	H

ϕ = DON'T CARE
C = $\bar{C}_E + C_C$
A clock H is a clock transition from a low to a high state.

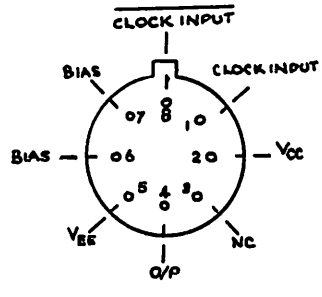
AD7531 - 4-Quadrant Multiplying D/A Converter



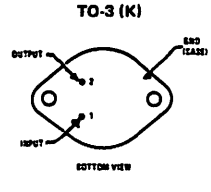
82S123 - 256-Bit Bipolar PROM (32 x 8)



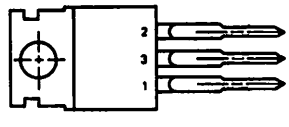
SP8659A - High Speed Divide by 16 Divider



LM309 - 5-Volt Regulator



7815UC - 15-Volt Regulator
7915UC - Minus 15-Volt Regulator



	7815UC	7915UC
2	output	output
3	common	input
1	input	common

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