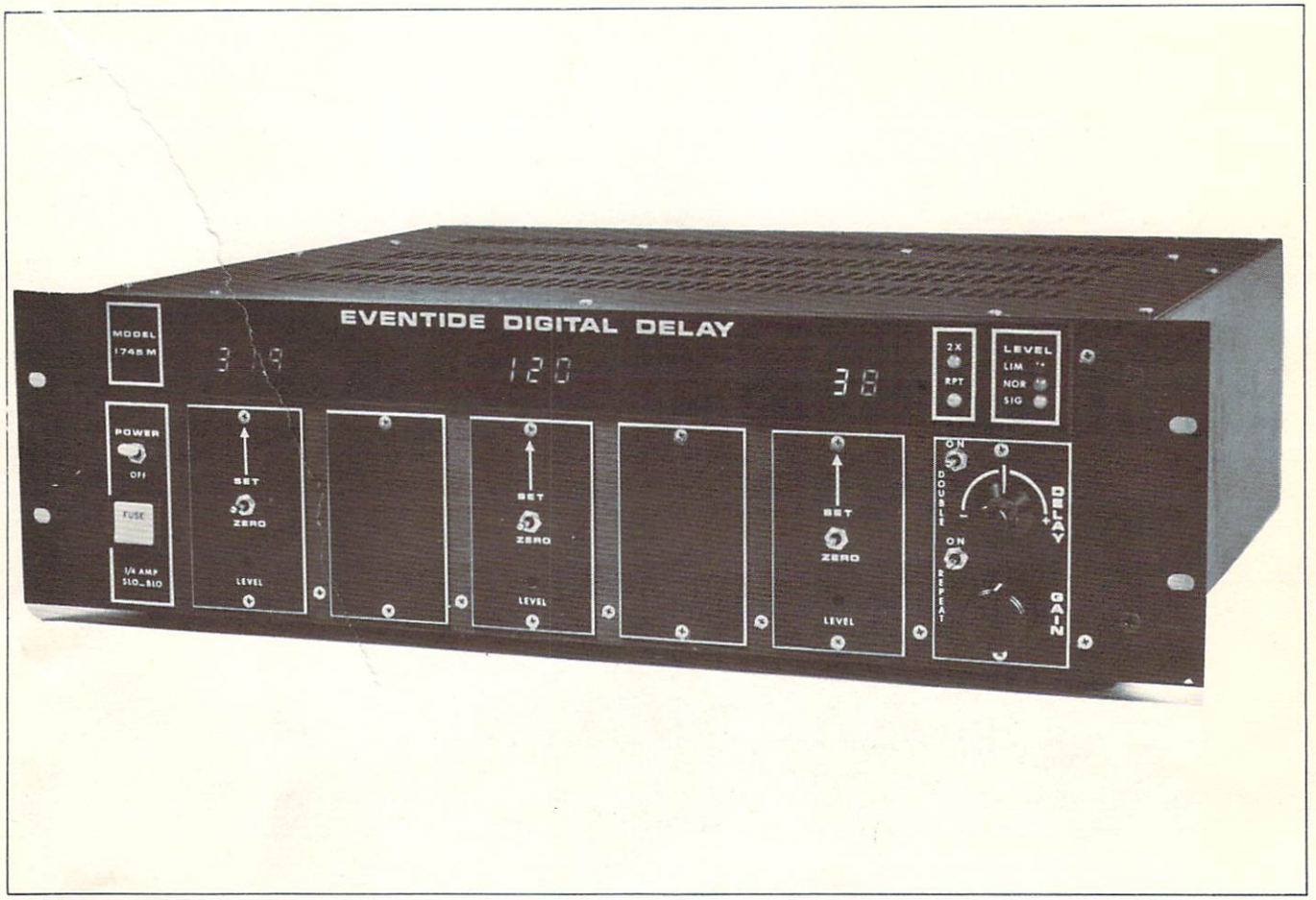
Eventide
the next step

INSTRUCTION MANUAL



DIGITAL DELAY LINE MODEL 1745M

LIMITED WARRANTY

THE EVENTIDE MODEL 1745M DIGITAL DELAY IS WARRANTED FOR A PERIOD OF 1 YEAR from the date of purchase from Eventide or an authorized dealer, against defects in material or workmanship. In case of difficulty, contact Eventide or your dealer for instructions.

This warranty does not apply to mechanical defects caused by use or rough handling, or to damage caused by improper operation not in accordance with this manual. Cause of defect is in the sole judgment of Eventide.

Much of the circuitry in the DDL is manufactured with static sensitive MOS and CMOS components. If you are requested to return a defective circuit card, this card MUST be wrapped in aluminum or other conductive foil. If this is not done, the warranty for the card in question is void.

The warranty is voidable at Eventide's option under the following circumstances:
user makes unauthorized modifications of any type; or,
the unit is connected to an improper voltage supply.

If the unit is modified by the customer without permission, the customer agrees to pay for any time or parts necessary to remove the modification before repair.

Eventide will under no circumstances be responsible for consequential damages caused by failure of equipments of its manufacture, or for any other reason. Our sole liability is for repair or replacement of the defective equipment under the terms of the warranty.

SHIPPING

Equipment should be returned, if possible, in the original packing container. Loose cards should be wrapped in conductive foil. If the original container is not available, the equipment should be packed to prevent damage from crushing and dropping. We recommend UPS over US mail, and air freight if you're in a hurry. If, in our opinion, the packing container is improper for return shipping, we reserve the right to supply a new container and charge for same.

The warranty covers return shipping by UPS within the continental US except Alaska. Return shipments will not be insured unless customer requests and agrees to pay for same. If a more expensive method of shipment is requested, the customer will be charged for the difference.

Foreign shipments must be returned fully prepaid, including customs and brokerage charges. Repaired equipment will be shipped all charges collect.

EVENTIDE CLOCK WORKS INC.

WARRANTY REGISTRATION FORM DIGITAL DELAY LINE 1745M

SERIAL NUMBER_____DATE PURCHASED_____

FROM WHOM PURCHASED_____

_____

NAME OF PURCHASER_____

ADDRESS_____

CITY_____STATE_____ZIP_____TEL_____

CONFIGURATION_____OUTPUTS_____TRANSFORMERS_____VOLTAGE

OTHER_____

THE 1745M is an expandable system and we would like you to know about new modules as they become available. To whom should this information be sent?
NAME

_____

Address _____

OPTIONAL-PLEASE FILL OUT IF YOU HAVE TIME

NATURE OF YOUR BUSINESS_____

APPLICATION FOR THE DDL. IF SOUND REINFORCEMENT, ADDRESS OF SITE_____

_____

_____

HOW DID YOU LEARN ABOUT EVENTIDE EQUIPMENT?_____

IMPORTANT: YOU MUST FILL OUT THIS FORM TO ENSURE WARRANTY PROTECTION!

A BUSINESS REPLY ENVELOPE IS PROVIDED FOR YOUR CONVENIENCE. FORM SHOULD BE MAILED WITHIN 10 DAYS OF PURCHASE.

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INSTRUCTION MANUAL MANUAL

Of necessity, this is an unusual instruction manual. Most audio engineers are familiar with audio equipment, and, of course, the Model 1745M digital delay line is a piece of audio equipment. However, except for a very small portion of the internal circuitry (the input and output amplifiers) the delay line will be unfamiliar to most people whose experience has been exclusively in the audio field.

Inside the DDL, many "state-of-the-art" technologies are employed. There are operational amplifiers, MOS RAM's (random access memories), analog to digital converters, CMOS integrated circuits, light emitting diodes and displays, binary to BCD and back again converters, and some rather densely packed double sided printed circuit boards (with plated through holes yet.) Although the design is straightforward, the schematics are replete with unfamiliar (to audio people) symbols and signals with names and strange properties.

Therefore, this manual is organized into two sections. The first section is the operating manual and contains data on what goes into the delay line and what comes out of the delay line: (audio, pure and simple). This section also contains helpful operating hints, application notes, and anything else which in our opinion will be useful to the engineer responsible for using the equipment. This section also contains a primer in the form of magazine articles which discuss in general form the technology behind the DDL.

The second section is the service manual. While we hope that the unit will not require servicing, we recognize that any device may fail, and more complex devices are more likely to fail than simple amplifiers or equalizers. The delay line rates as a complex device, containing as it does on the close order of 200 integrated circuits, many of which are are the equivalent of over ten thousand transistors! If that is not impressive, consider a pile of transistor radios the size of the great pyramid of Cheops. That *is* impressive. Irrelevant, but impressive. The service section contains complete technical information about the delay line, including schematic and block diagrams, theory of operation, troubleshooting suggestions, and an appendix. The appendix purports to teach some of the rudiments of digital troubleshooting to engineers familiar with audio techniques, but unacquainted with digital technology.

Copies of Section One are supplied with relative abandon, both with rental units and to prospective purchasers. Copies of Section One may be purchased for $2.50 each, refundable on purchase. Copies of Section Two are serialized and zealously guarded by a battery of white-lipped attorneys fallen on hard times. The timberwolves were released when the price of flesh exceeded the price of food. Additional copies of Section Two may be purchased for $25.00.

This manual covers the standard 1745M delay line, which contains the basic complement of circuit cards. Additional cards will be brought out from time to time, and information about these optional cards will be contained in separate addenda. Information on adding additional standard outputs is contained in this manual, however, and no additional manual is required when ordering them.

SPECIFICATIONS: MODEL 1745M

INPUT LEVEL	Adjustable by front panel control. -10 to +16dbm nominal for full output level as evidenced by illumination of red LIMIT indicator
OUTPUT LEVEL	Clipping level +18dbm. Screwdriver adjust control accessible from front panel available for small adjustments.
IMPEDANCES	INPUT balanced electronically, each line nominal 4.7K in series with 1000pf to ground. 600 ohm xfmr optional. OUTPUT unbalanced, 150 ohms nominal. Transformers are optional, and increase maximum output to +22dbm. Without transformers, input should not exceed 40V p-p, or ±12V p-p on either line.
FREQUENCY RESPONSE	±1db, 30Hz-16kHz. Extremely rapid rolloff after 16kHz.
DISTORTION	Less than .3% THD from just below clipping to -10dbm output between 100Hz and 10kHz. Less than 1% over remainder of frequency range.
DYNAMIC RANGE	Greater than 90db between minimum usable signal and clipping level. Solid state indicator flashes red nominally 3db below clipping, green nominally 12db below clipping, and yellow when signal is present.

DELAY CHARACTERISTICS

DELAY	Variable in 20 microsecond steps to 319.98 milliseconds. Variable in 40 microsecond steps to 636.96 milliseconds in DOUBLE mode, reduced frequency response.
DELAY MATCH	When outputs set to identical delay, adjacent output relative delay less than 3us.
MINIMUM I/O DELAY	Less than 40us.
SHORT TERM STABILITY (wow and flutter)	.001% (1 part in 10^5 averaged over 100 ms interval)
LONG TERM STABILITY	.01%/month.
ACCURACY	Readout accurate to nearest millisecond. Optional readout gives delay to nearest 10uSecond. Accurate to .02%.

PHYSICAL CHARACTERISTICS

HEIGHT	13.34cM (5-1/4")	standard rack dimension*
WIDTH	58.26cM (19")	standard rack dimension
DEPTH BEHIND PANEL	38.10cM (15")	

*Normally supplied with rubber feet for tabletop mounting. Feet may be removed for rack mounting.

POWER REQUIREMENTS	115VAC, 50-60Hz, nominal 25VA. May be internally wired for 230VAC, 50-60Hz.

INTERCONNECTION

The 1745M is capable of containing 1 INPUT module and up to 5 OUTPUT modules.

Each module position is represented on the rear panel by one 3-conductor audio connector. These connectors employ the following wiring convention:

BALANCED CONFIGURATION

	INPUT	OUTPUT
PIN 1	Connected to analog ground	Connected to analog ground
PIN 2	Input, -phase	Output, -phase
PIN 3	Input, +phase	Output, +phase
IMPEDANCE	Either HI or 600 ohms depending upon input resistor	600 ohms

UNBALANCED CONFIGURATION

	INPUT	OUTPUT
PIN 1	Connected to analog ground	Connected to analog ground
PIN 2	Input, -phase	Connected to analog ground
PIN 3	Input, +phase	Output, +phase
IMPEDANCE	HI	150 ohms.

Input connector is female type D3F. Mating cable connector is type A3M.
Output connector is male type D3M. Mating cable connector is type A3F.
Part numbers are Switchcraft. Equivalent connectors are made by Canon and others.

DISPLAY BRIGHTNESS

The delay line is furnished with the displays set at what we believe to be optimum brightness for typical studio applications. The display brightness can be increased or decreased by about 50%.

To INCREASE BRIGHTNESS: Remove DDL top cover and place shorting link across diode in series with PIN V of the readout board socket.

To DECREASE BRIGHTNESS: Remove DDL top cover and connect additional diode in series with diode going to PIN V of the readout board socket.

Caution: Do not decrease brightness by more than one diode to prevent marginal operation of decoder IC's.
Do not increase brightness if more than 3 outputs with readouts are installed to prevent possible power supply overload.

MAIN FRAME

The POWER switch is the only control not associated with a particular plug-in module. This control applies AC power to the entire unit.
The FUSE receptacle is connected in series with the POWER switch and an additional internal fuse. To protect the unit, the correct fuse must be installed, as per the following table:

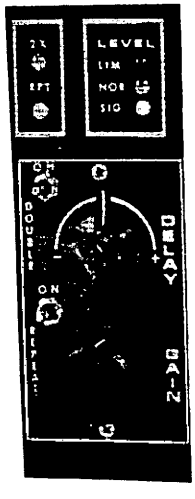
VOLTAGE:	115VAC	230VAC
INTERNAL	3/8Amp	3/16Amp
EXTERNAL	1/4Amp	1/8Amp

To replace the fuse, press the bottom of the insert until the top pops forward.

INPUT MODULE CONTROLS AND INDICATORS

The GAIN control is used to adjust the input level to the delay line. Full clockwise rotation allows signals of approximately -10dbm to achieve full dynamic range. Full counterclockwise rotation cuts off the input signal.

The three colored light emitting diodes in the LEVEL block on the Plexiglas panel indicate the relative input level. The RED lamp becomes illuminated approximately 3 db before the input signal reaches the clipping level (LIMit). The GREEN (NORmal) lamp becomes illuminated approximately 12 db before the input signal reaches the clipping level. The YELLOW SIGnal present lamp becomes illuminated when there is any significant signal applied to the input.



The spring return REPEAT switch allows the signal present in the delay line's memory to be captured and repeated. Momentarily deflecting this control upward activates the feature, and momentarily deflecting it downward de-activates the feature. An orange RPT light emitting diode in the Plexiglas panel becomes illuminated when the DDL is in the REPEAT mode.

The spring return DOUBLE switch causes the input sampling rate to be cut in half by discarding alternate samples. This halves the rate at which data are written into the memory, and thus doubles the total delay time. An orange 2X light emitting diode in the Plexiglass panel becomes illuminated when the DDL is in the DOUBLE mode. When this LED is on, the correct delay of each output is equal to twice the amount indicated in the associate readout. The switch operates in a manner similar to the REPEAT switch: press up to activate, down to de-activate.

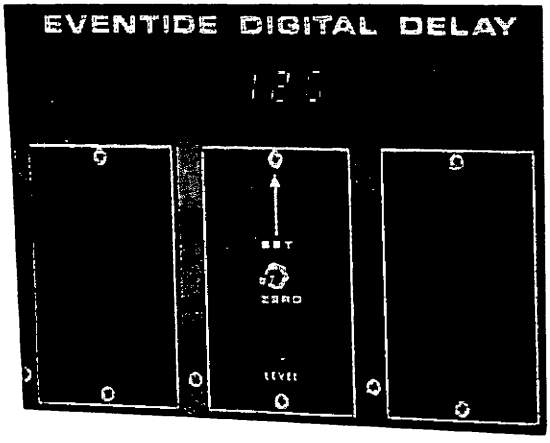
The DELAY control activates a wide range oscillator which switches the delay in small steps, one step per pulse. This oscillator is disabled when the knob is aligned with the arc divider. As it is rotated in either direction,

the oscillator frequency increases logarithmically. At the extremes of rotation, pulses are produced at a rate sufficient to traverse the entire delay length in approximately 3 seconds. At the slowest setting, the delay varies at about 1 step per second. A graph showing the control setting *versus* delay change rate is shown at left.

A steering signal is also produced by the control which determines whether the delay is to increase (CW rotation) or decrease (CCW rotation).

The delay change process is nearly inaudible, except at the extremes of rotation, at which point the output signal appears to suffer a pitch and tempo change. In order to get a feeling for the action of the control, it is recommended that the instructions in the FLANGING application section be followed.

OUTPUT MODULE CONTROLS AND INDICATORS



Each output module has facilities for independent delay adjustment (under control of the DELAY control described above) and level.

The switch marked SET/ZERO tells the module to accept the oscillator signals when in the SET position, or to ignore them in the center off position. Each module may be set independently by placing the switch in the SET position, adjusting the delay with the DELAY oscillator and then centering the switch and proceeding to the next module.

Each module may be independently ZEROED by momentarily deflecting the switch downward. (This is a spring-return position.)

Each module has power-up-clear circuitry to reset the delay to zero upon application of power. If more than one module is in the SET position and the DELAY control is not centered when power is turned on, it will be noted that, after a short delay, the outputs will begin to count. Because there is a time delay involved which is different for each module, the outputs will not track precisely, nor should they be expected to. In general, the outputs will only track precisely when they have been in the SET position the same amount of time, and subject to the same number of oscillator pulses. It requires 50 pulses for the readout to change by 1 ms.

The readout indicates, to the nearest millisecond, the delay at which the output is set. If the delay is less than 10 milliseconds, only one digit is illuminated, if less than 100 milliseconds, only two digits are on. The readout will reset above 319 to 0, and below 0 to 319.

INPUT LEVEL SETTINGS

The Eventide Digital Delay Line is similar to amplifiers, equalizers, tape recorders, and virtually every other electronic device with the possible exception of a piece of wire at absolute zero in that it has a certain, limited, *Dynamic Range*. Dynamic range is defined as the levels between which operation of the of the device in question is useful or acceptable. As a practical matter, the range is usually bounded on the high side by excessive distortion, and the low side by excessive noise. In many equipments, a level indicating device such as the familiar VU meter is provided to indicate when the unit is operating at the proper level. A tape recorder, for instance, has a certain percentage of distortion at OVU, and this percentage rapidly increases as the signal level increases. The noise level is some number of decibels below OVU. This number of decibels is defined as the DYNAMIC RANGE.

Signal sources typically have a dynamic range much greater than that of electronic devices. Likewise, the ear can hear a dynamic range much greater than that of electronic devices. Since the electronic device (the Delay Line in this case) is the limiting factor, it is obviously a good idea to set the operating level of the delay line to take advantage of the maximum dynamic range of which it is capable. This is the equivalent of making sure that the meter on a tape recorder is reading around OVU most of the time.

To enable accurate setting of input level, three solid state lamps have been provided on the front panel. The lamps are arranged in a column, yellow on the bottom, green in the middle, and red on the top. The DDL is adjusted internally so that, at 1KHz input frequency, the red light will come on nominally ½ db below the point at which both the analog and digital portions of the unit approach the clipping level. This corresponds to an analog signal level of about +14dbm into 600 ohms. A momentary red flash of the indicator shows that the system dynamic range has been momentarily approached or exceeded. Continuous operation of the red indicator on program material is indicative of severe distortion.

The green light will come on at a level approximately 12db below the clipping point, and indicates the normal signal range at which the delay line should operate.

The yellow light comes on when any signal is present, even at a very low level. This is an aid in making sure that the unit is properly connected, and that a signal is present. It will be on almost continuously during proper operation.

ALTHOUGH THE RED LIGHT INDICATES THAT THE DELAY LINE IS ON THE VERGE OF CLIPPING, IT IS DESIRABLE TO OPERATE THE UNIT WITH THE RED LIGHT FLASHING INTERMITTENTLY!

The internal signal processing circuitry assures that, with normal program material, intermittent flashing of the red light does not mean that the signal is being significantly distorted. This is important to understand, because most signals will have some peaks which are much greater in amplitude than the average level, and attempting to preserve these peaks faithfully results in a serious compromise in dynamic range. In operation, it will be found that the red light flashes more frequently as the DDL is connected closer electrically to the microphone, and that it can flash more fre-

quently when so connected before the distortion becomes objectionable. This is so because other equipments in the audio chain have similar peak clipping properties. (And, of course, the ultimate limiting factor is the tape or disk.)

When the GAIN control is properly adjusted, the green light will be on most of the time, and the red light will be flashing intermittently. This flashing may be anywhere from several times per second to once every few seconds. The table below gives a rough indication of proper settings.

INPUT LEVEL SETTING CRITERIA

TYPE OF SIGNAL AND SOURCE	YELLOW DUTY CYCLE	GREEN DUTY CYCLE	RED DUTY CYCLE
Integrated program (radio)	100%	80%	once per 2 sec
Integrated program (live mix)	100%	50%	once per second
Voice (talking)	75%	30%	once per 2 sec
Piano	100%	30%	2-3 per second
Guitar, acoustic	75-100%	30%	2 per second
Guitar, fuzz	100%	60%	1 per second
Synthesizer	80%	80%	infrequent
Organ	80%	80%	infrequent
Drums	75-100%	20-70%	once per well-defined beat.

All the above numbers are approximate. They will vary widely if the signals are pre-processed through limiters, equalizers, or any other amplitude-distorting processor.

In general, it is not necessary to be very critical about the level setting, any more than it really matters if you record at +1 or -1. However, it is always good practice to get the most from your equipment, and the above settings will give you the most dynamic range. For most applications, the DDL's 90db dynamic range will not be the limiting factor in the signal chain.

DELAY DOUBLING

As much as we'd like to, we cannot furnish a 640 millisecond delay line for the price of a 320 ms unit. There ain't no such thing as a free lunch, and RAM's cost more than munchies. We can, however, do the next best thing: We have put a switch on the front panel which says "DOUBLE", and turning this switch will double the delay capacity of the 1745M. *BUT*, at the same time, the frequency response is degraded. In other words, in the DOUBLE mode, we do not consider the 1745M to be a studio quality unit.

The reason for this degradation is inherent in engineering arcana known as "sampling theory", discussed a bit more technically later on. Suffice it to say that the DDL looks at the incoming signal at a certain rate known as the "sampling rate", and transmits these samples through a delay to the output. In the DOUBLE mode, alternate samples are ignored and are not sent to storage. Since the storage capacity remains constant, it is only filled half as fast, and so will store the signal twice as long, thus doubling the delay. However, since the samples are taken less frequently, anything occurring between samples (*i.e.*, during the sample which was ignored) is discarded. In practice, this means that high frequency signals greater than about 10kHz are subject to heterodyning and various forms of distortion. High frequency sine wave tests produce truly weird results. Fortunately, normal program material does not contain high frequency sine waves and so is only slightly modified. The major difference between modes shows up as a harshness in the treble register. Much of this can be eliminated by EQ'ing down the highs on both input and output, at the further expense of frequency response.

Don't let the foregoing scare you into not using the delay doubling feature. Despite the harshness, program quality is perfectly acceptable except for fairly critical listening. Speech, especially, is relatively unaffected by delay doubling, as are other signals which do not have a large high frequency content.

APPLICATIONS

The DOUBLE provision is primarily of use in instances where greater than 320 milliseconds of delay is required and less than optimum quality can be tolerated. Sound reinforcement applications particularly suggest themselves due to the normally present high frequency attenuation of the atmosphere, and the fact that it's rarely possible to listen critically to a PA speaker. The harshness at high frequencies will usually be inaudible if there is any masking signal present.

Other applications which suggest themselves are special effects and communications uses in which the signal channel parameters will be more limiting than the DDL response. Many of the uses of the DOUBLE mode occur in conjunction with the REPEAT mode. For instance, a signal can be "captured" in the DOUBLE mode and then recirculated in NORMAL. If this is done, it will be played back twice as fast, for a nice Mickey Mouse effect, or a substantial aid to spectrum analysis and voice printing. Further applications will be discussed after the recirculation section of this manual.

The Digital Delay Line

REVISITED

Remember when the Digital Delay Line was new? You don't have to go back too far in the audio business to remember the first DDL, complete with such exotic concepts as an Analog to Digital converter, magnetostrictive delay lines, anti-aliasing filters, and such marvelous arcana as *bits* and *clocks* (which didn't even tell time).

Well, if you've been awake in recent years, you know a bit about digital technology by now. Your watch is digital, you have a digital calculator (or pocket computer for a few extra bucks), your voice is frequently digitized on the telephone, your tape machine searches digitally, and you may have even learned to count on your fingers. Of course, if you've done any mixing or sound reinforcement work, you've undoubtedly used a digital delay line for the special effects or time synchronization of which it is uniquely capable. Somewhat less likely, you've had occasion to delve into the electronic circuitry by which these units achieve their delay. The DDL is "transparent" to the end user, i.e., an audio signal goes in, and an audio signal comes out somewhat later. Absent curiosity or malfunction, there is no need for the user to know what goes on inside the unit. Ask a non-technical person what is going on inside a DDL, and he will probably make some reference to Analog to Digital converters, Shift Registers, and Digital to Analog converters. Don't ask any further questions as they will probably lead to mild embarrassment. They needn't, though, because that last sentence is a fair summary of what really does go on in a DDL. After a brief flirtation with magnetostrictive delay lines (very clumsy mechanical delay lines), the industry universally adopted the integrated circuit shift register as its method of storing signals to be delayed.

Very briefly, the principle of operation of the DDL is this:

1: An audio signal is low-pass filtered to eliminate super-audible signals which could cause beat notes and spurious outputs.

2: The signal is then converted into a digital format at a rapid rate, typically 25 to 50 thousand times per second. Each of these 25K to 50K *samples* is represented by a digital *word*, which consists of a group of "1's" and "0's". The word represents a specific voltage level as present in the original signal.

3: This word is *clocked* into a digital storage medium, such as a semiconductor shift register, in which it is progressively moved towards the output, one storage location per clock or sample period. The delay is thus determined by the clock rate and the number of storage locations available by the rather simple relationship

$$\text{DELAY} = \frac{\text{Number of storage locations}}{\text{Clock or Sampling frequency}}$$

4: After the digital word reaches the output of the shift register, it is reconverted to an analog format and again filtered to remove spurious frequencies, this time primarily associated with the sampling clock.

5: The signal, thus converted and delayed, is conducted to the outside world, ready to begin its career.

The above admitted oversimplification completely ignores the differences between delay lines from different manufacturers, which are primarily related to methods of encoding the analog signals into digital format, and the various control features of the competing units. The method of signal processing determines the dynamic range of the unit: depending upon the application, ranges of from 40db to over 90db are desirable, and it makes little sense to purchase more range than required because the cost is directly proportional to the dynamic range, as both the amount of storage and circuit complexity increase with increasing dynamic range. Likewise, units are available with delay switchable in narrow increments with great facility, to those in which delay is completely fixed at purchase. Naturally, you pay for control features, and for delay time. The third major trade-off is frequency response. Within narrow limits, the frequency response is about 1/3 the sampling rate. Doubling the sampling rate doubles the rate at which the digital samples pass through the shift registers, and thus cuts the delay time in half. So, one would expect a given delay line to give half as much delay at 50kHz as at 25kHz. It is possible to compromise, however, so that a given delay line may have variable or selectable clock rates to allow longer delays when wide frequency response is not necessary, such as in some special effect or sound reinforcement applications.

With all these differences, there has been one unifying and limiting factor in DDL design: All units have used the shift register as a storage medium. To see why this is limiting, let's look at the shift register:

The shift register is a *serial* storage device. It comes in various lengths, from 4 bits to several thousand bits. New technology has recently made 16kilobit registers possible. At first glance, it would seem that shift registers are ideal for delay, because of their very structure. They work by transferring a packet of charge representing a digital 1 or 0 from one internal node to the next. No additional timing circuitry is necessary-the registers accomplish the delay all by themselves. Furthermore, they may be connected in series to achieve longer delays, and the points at which they are connected can be used as delay taps. If each shift register provides, for example 10 milliseconds of delay, and 20 are connected in series, 200 milliseconds are available in 10 millisecond steps. As a practical matter, many parallel shift registers are required to handle a full word, and the switching becomes cumbersome after a few taps are necessary. There are many techniques for circumventing this problem which add only minimal complexity to the entire system. So what's the problem? Well, consider how to vary the time delay. There are two basic choices: one is to switch shift register taps; the other is to vary the clock rate. Switching taps creates discontinuities in the signal. Looking at a signal at point A and point B at, say, 1 millisecond time difference creates a sharp transient at the splicing point (see figure B). Even if the switching is accomplished electronically, such as with an optical encoder and digital multiplexers, this transient is unavoidable, except when the signal level is zero, or the points to be joined coincidentally have the same amplitude. If the delay is to be changed rapidly, this becomes a serious detriment, as many of these splices add noise to the signal. Varying the clock rate overcomes this problem, but creates another one, the inability to vary the delay by more than a certain percentage. The upper limit of variation is governed by the allowable decrease in frequency response; the lower limit by the capability of the A to D converter and the timing circuitry. A typical variation of 50% is insufficient to change from short to long delays, and since all outputs vary by the same percentage, it is impossible to vary one output with

respect to the other. The basis of the flanging effect is the sliding of one signal past another in time, and so this lack of capability is a great disadvantage.

One solution to the above problems would be to have shift registers with taps every sample. So doing would enable one to switch from tap to tap rapidly while encountering only insignificant splicing noise (Fig. B). This is because, with normal program material, the amplitude difference between successive samples is very small. Switching between samples in this manner produces at worst a low amplitude tone at the switching rate which is effectively masked by the signal. The only time you run into trouble with this method is varying the delay of high frequency deterministic signals, which is very unlikely in normal circumstances. Unfortunately, tapping shift registers at every bit would require a maze of wiring large enough to fill an ordinary city dump, and the equipment would end up there after one repair was attempted. (It is possible to use combinations of shift registers to achieve an arbitrary delay time, but this is not the same and will not work, just in case anybody is tempted to try. The reason it won't work is that in switching individual shift registers around, it becomes necessary to wait for them to fill up, which can take an arbitrary length, much greater than one sample, before the output is usable.)

Another solution to the above problem is to use Random Access Memories. This solution does work, and is described starting now.

Description of Random Access Memories

A random access memory is a semiconductor chip (or assemblage thereof) which can store individual chunks of data, and deliver them up upon command. They differ from the shift register in that any of the stored data is immediately available regardless of when it was entered into the memory. If the shift register is compared to a pipeline, the RAM may be compared to a book, in which each page is numbered and accessed without reading its neighbors. In digital terminology, the "page numbers" are "addresses", and an individual RAM integrated circuit may have from 16 addresses, as used in either very old or very fast chips, up to 4096 addresses as used in many of the newest computers. Assuming each address location holds 1 bit, it is obvious that one "4KRAM" is the equivalent in storage capacity of four industry standard 1K shift registers. Of course, nothing exists in a vacuum, and the 4KRAM must be economically viable, available, and reliable. Fortunately, this is the case, as the price of the 4KRAM, which was astronomical until mid 1975, is now in the range where it is reasonably comparable to the price of the shift registers which it replaces. Anticipating the price reductions, we began the design of a Digital Delay Line using random access storage instead of shift registers. Some of the details of the design, and the possibilities of RAM's are described below.

To begin with, getting delay from a memory is a bit more involved than getting delay from a shift register. To allude to the book vs. pipeline analogy, if you put something into a pipeline, you need only wait for it to come out. The delay is equal to the length of the pipeline. If you wanted to get delay from a "book", you would have to read the data a certain number of pages after the beginning. Since this is a dynamic process, the point at which the data are written also must vary. (If it did not, data would be overwritten at the same location. Look at an old piece of carbon paper and try to imagine what that would *sound* like!) Therefore, the way to get delay from a memory is to employ a *pointer* or *base address* register. Every time a new sample is written into the memory, the register is decremented (decreased by 1). This register then points to the location of the

most recently written data. Since the register is decremented once each sample period, adding 1 to the register contents points to a sample that is delayed by a sample period. If the sampling rate is 50KHz, then, each sample is 20 microseconds delayed from the previous one, and if data are being written at address #150, then data being read at address #200 are delayed by 1 millisecond. Fortunately, the actual numerical address is irrelevant, as all data storage locations are identical. Thus, an output can be obtained at an arbitrary delay simply by generating a number equal to the number of samples difference between input and output. The "housekeeping" is taken care of by a single register and arithmetic unit located on the circuit board which contains the memory.

Most delay lines, especially those used in recording studios, have two or more outputs. Multiple outputs are especially desirable in those applications involving choral effects and reverberation. In order to accommodate multiple outputs, it is necessary to organize the system as a "bus", which means simply that several different signals can share the same physical connection. Doing this requires "3 state" logic, which differs from ordinary 2 state digital circuits in that not only can a 1 or a 0 be output, but the output also can be turned "off", in which case it assumes a high impedance. If multiple outputs are connected together, but only one is in a low impedance state, then the bus assumes the state of the low impedance output. By using modular output cards, and activating them sequentially, one can access several different addresses during any given sampling interval. The number of addresses which can be accessed is determined by the "access time" of the memory chip used and the sampling interval, which as stated above is 20 microseconds. Most common 4KRAM's have access times on the order of .2-.4 microseconds, which should be sufficient for 50 to 100 outputs. However, computing the proper address also requires time, and common TTL circuits, which are very fast, consume quite a bit of power. As one of the objectives of the design was to reduce power consumption, we used all CMOS circuitry, whose power consumption decreases almost to zero as its speed decreases. Even so, there is plenty of time to service up to seven outputs, and module positions are provided for up to five, leaving margin for extra functions.

Another problem arises in that RAM's are universally binary devices, and human beings are generally decimal. Some provision must be made to allow setting the delay (and reading it out) in human-decipherable units. Since each sample is 20 microseconds, one could simply convert the binary number representing the delay to decimal form and multiply by .020 to give milliseconds. Unfortunately, long binary to decimal conversions are slow or require much hardware. A far simpler solution involves using a small (0 to 999) decimal to binary converter, and doing all the output module addressing in decimal form. Each 4KRAM has binary addresses from 0 through 4095. Then memory locations 0 through 999 (binary) are addressed for the first 1000 samples of delay. If 1001 samples of delay (20.02 milliseconds) are required, the next address used would be binary 1024. In effect, for convenience, 96 addresses out of every memory are ignored and wasted. These addresses are still there, by the way, if needed, but it is a lot cheaper to waste them than to perform the conversions otherwise required. Using this system and sampling rate, a 16K memory, requiring 40 memory chips gives 319.98 milliseconds of delay in 20 microsecond steps, as compared to our previous system requiring 108 shift registers for 199 milliseconds, in 1 millisecond steps. A small additional advantage is that no extra shift registers are required for additional outputs. Assuming comparable reliability between the RAM's and shift registers, the memory design should be over twice as reliable. Furthermore, the industry has settled on two or three basic 4KRAM designs, and all are multiply sourced. We opted for the 22pin, non-multiplexed address configuration for simplicity, and because space saving was not an urgent criterion. We have evaluated several manufacturers chips and found all but one acceptable. This, hopefully, will make delivery times independent of

Silicon Valley idiosyncrasies.

One final unusual design feature: our 1745A delay line utilized an optical encoder (see January 1974 db magazine) for delay switching. This eliminated the need for coarse and fine delay controls and permitted fully incremental switching in 1 millisecond steps. The control had 20 lines, and produced 20 pulses per revolution, and could be spun to traverse the whole control range in one spin. To do the same with a unit which varies in 20 microsecond steps would require an encoder with 1000 lines. Although such devices are producible, and are used in precision mechanical systems, it was deemed impractical for reasons of cost and ruggedness. Instead, we designed an oscillator of wide frequency range with a small deadband in the center of its control range, and with parabolic control taper. The oscillator frequency range is from 1 Hz to 5kHz, which allows the full range of delay to be spanned automatically over several seconds to several hours. It should be noted that although the delay varies in 20 microsecond steps, the readout is only to the nearest millisecond. If one needs to know the precise delay, the information is available on data lines which may be connected to readout drivers. Other features of the 1745A were duplicated in relatively uninteresting ways. The delay double feature which allows doubling the delay at the expense of frequency response was implemented by inhibiting alternate base address decrementing pulses. The repeat feature was implemented by inhibiting memory write pulses, thus preventing over-writing old data and so saving them.

Superficially, then, we have a new delay line with a bit more delay and a whole bunch of familiar features implemented in a wholly new way. As stated earlier, the delay line is and should be transparent to the user in that, regardless of the implementation, you put audio in and get audio out. What does all this mean to the user?

Nobody would waste time with RAM's if it didn't mean something: of that you may be sure. It means:

That true flanging can be accomplished with a single digital delay line. The fine delay steps allow sweeping a variable output past a fixed output in tiny increments, thus giving an apparent continuous variation in tonality, as opposed to the step variations possible with other systems. Unlike analog delay flangers, the flanging may be performed after any fixed delay. Even "pre-flanging"is possible with a single delay line, by taking the flanging effect from the first two outputs and the dry signal from a third at greater delay. Of course, as with all digital systems, there is no degradation of signal to noise ratio as the delay is increased.

It means:

That continuous doppler shift or pitch change may be introduced into any signal simply by increasing or decreasing the delay in a continuous fashion (facilitated by the oscillator control). A rather long period of change is available before an artifact is introduced by the delay recycling from 319 milliseconds back to zero, and this can be minimized in certain ways involving interleaving more than one output.

It means:

That an auxiliary module which computes addresses in accordance with an appropriate program can be used to obtain an arbitrary pitch change ratio, and maintain that ratio. ANY ratio can be obtained. By proper address manipulation, it is possible to read audio out backwards! Think of that, special effects fans! And of course pitch change can be turned into tempo change in conjunction with a

tape player.

It means:

That precise comb filters may be implemented with much finer control of delay. Since the system is crystal controlled, the delay time will not drift more than a few parts per million, and so a null can be set for some frequency and that frequency and its harmonics will be disappeared.

And that largely experimental applications, such as narrow bandwidth speech scrambling can be reasonably implemented. For instance, construct a card that will read out addresses 0 to 1000 normally, then jump to 5000 to 6000, then readout 2000 to 1000 backwards, etc, until the whole capacity is used up! Performing the inverse operation at a remote end will descramble the signal. The whole process, unlike digital encoding, does not significantly increase the bandwidth of the output, and thus it may be put on ordinary communications channels such as the telephone. This may also be an aid to communications, by using the memory delay line in conjunction with several filters, and setting each filter band at a different time delay. This is known as time-diversity transmission and can also be implemented with non-memory delay lines, but sure fits in with this paragraph.

And that experimental applications requiring digitized audio be available at various times can be implemented with a convenient test bed. Computer time need not be taken up implementing A to D routines and housekeeping. Samples may be withdrawn at any computed delay and used as the experimenter desires.

In addition to the above advantages, there is another capability built in to the system as a consequence of the memory bus architecture. If one can hang several outputs on a given bus, why not several inputs as well? Why not indeed! In fact one can, and so we did. The delay register inputs, normally set sequentially by the oscillator, can be set in parallel by placing the desired number on the address bus and strobing the output card which the engineer wants to set in the "dead time" between the last readout and a new sample. Provision has been made for a remote control module which enables precise setting of any or all outputs by digital control. Data may be furnished either from a remote console or from an automated mixdown system. Thus, another component can be operated in conjunction with automation, leaving the engineer and producer even freer to *listen*.

FIGURE A: STANDARD DELAY LINE BLOCK DIAGRAM

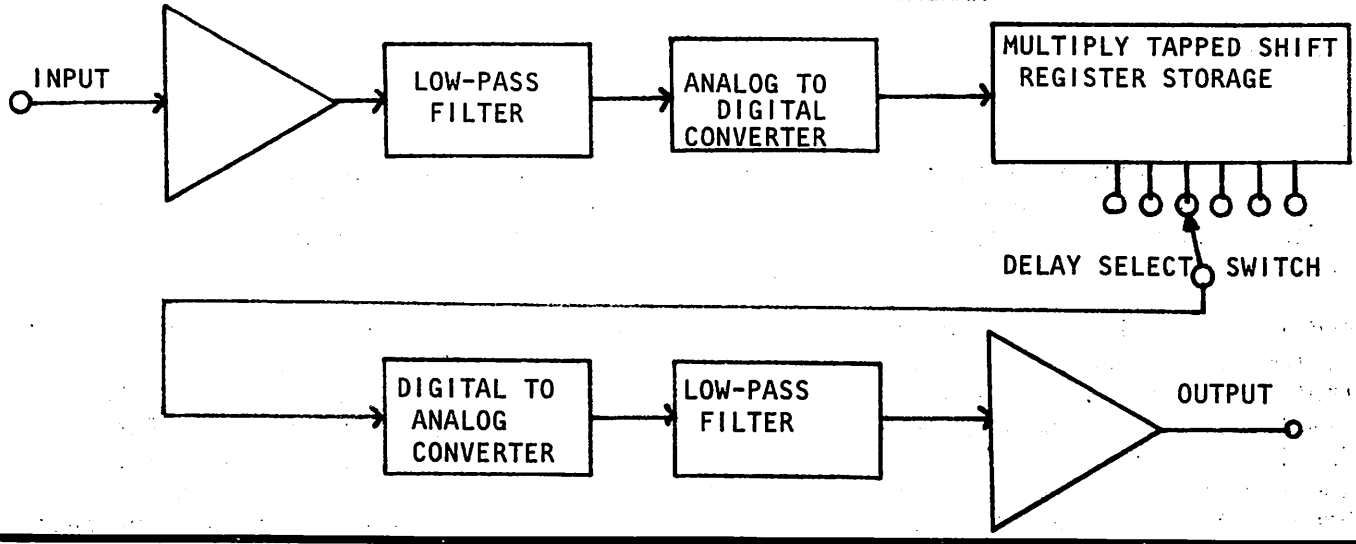
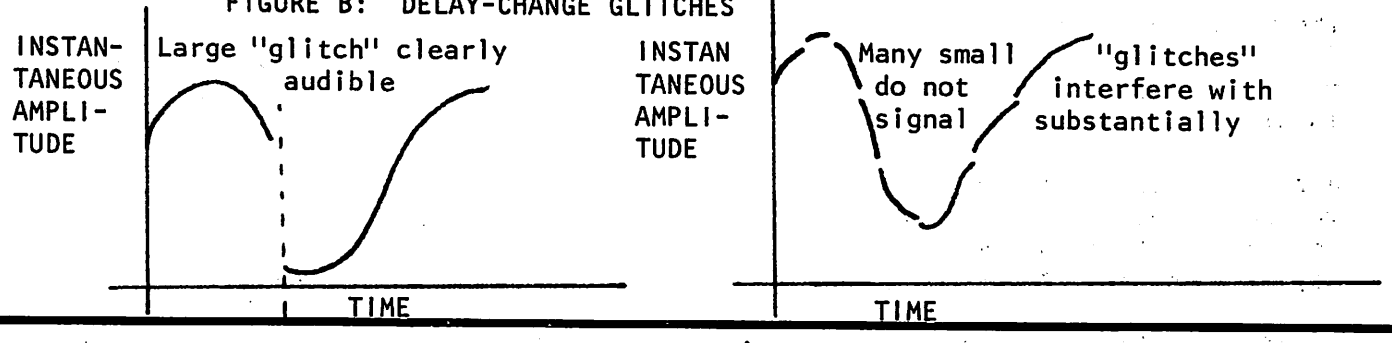


FIGURE B: DELAY-CHANGE GLITCHES



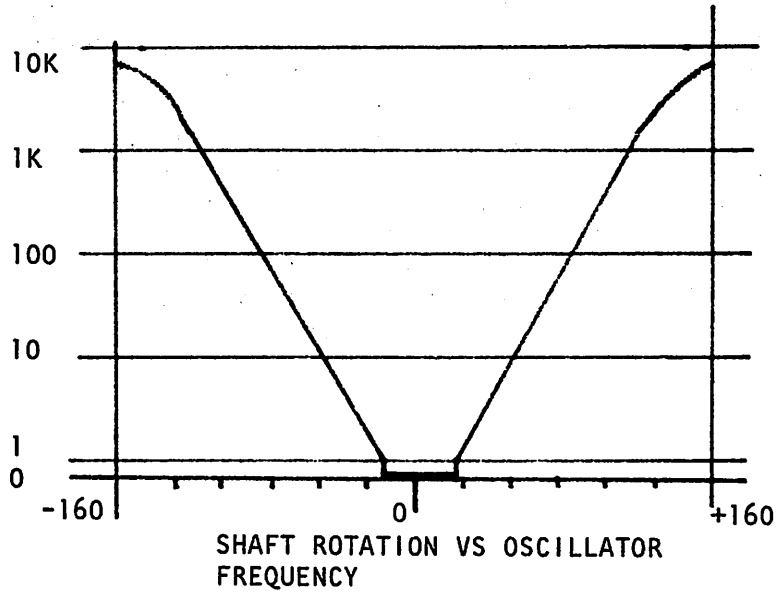


FIGURE C:
DELAY CHANGE CONTROL OPERATION

ARTICLE ILLUSTRATIONS

COMB FILTERS
RECIRCULATION
FLANGING
TUNNELING
PITCH CHANGING
AND GENERAL WEIRDNESS

If you think that you just bought a delay line, think again.

In addition to delay, the unique control features and system architecture of the 1745M allow you to do all sorts of strange and wondrous things to your unsuspecting signals. The title of this page is a good beginning.

C O M B F I L T E R

A comb filter is a device which has many frequency rejection notches or many peaks. Generally, these notches or peaks are evenly spaced , in a manner similar to the harmonics of a non-sinusoidal signal. A rudimentary comb filter can be made with a set of filters each adjusted to a different frequency, but this quickly becomes prohibitive, both in terms of cost and stability. A typical comb filter application is the rejection of interference in a broadband system. For instance, consider the case in which a tape made on location somehow picked up a tremendous 60Hz component. If only 60Hz is present, it can be nulled with a notch filter. More likely, however in addition to the 60 Hz, there will be 120Hz, 180 Hz, 240Hz, etc. components. SCR noise is notorious for causing such problems. Removing such noise from a tape can be accomplished with a comb filter.

The basis of the comb filter is that, if a signal is added to a delayed version of itself, a regular pattern of nulls and peaks in the frequency domain is produced. (See graphs and scope photographs). The reason for this is intuitively clear: Assume a delay of 1 millisecond. Apply a 1kHz signal to the delay line input, and algebraically add the input to the output. Since the length of a single cycle of 1kHz signal is 1 ms, the input and output are in phase, and a 6db addition results. Now apply a 500Hz signal to the input. The output will be delayed by ½ wavelength, and out of phase addition will result at every point on the signal, creating a null in response at 500Hz. The amplitude at any frequency can be calculated by the following formula:

$$H = \frac{\cos\frac{(T_d)\ (360)}{1/f} + 1}{2}$$

Where:
f is frequency in Hz
T_d is the delay time in seconds

To null any given frequency and all of its harmonics, the delay time should be set equal to 1/F, and the input and output added out-of-phase.

To null any given frequency and all of its odd harmonics, the delay time should be set equal to 1/2F, and the outputs added in-phase.

The 1745M delay line is excellent for comb filter use, because it is adjustable in extremely small steps, all of which are crystal controlled and consequently stable typically to a few parts per million per day. Several outputs can be combined with different "weights" and different delays to establish different filter characteristics, including highly desirable narrow notches, which will null out given signals with very little effect on the broadband signals.

RECIRCULATION

A unique feature of the Eventide Digital Delay Line is its ability to "capture" a signal in its memory and to continuously repeat this signal through the outputs. Since the signal is stored digitally, there is no decay or noise build-up as would be present if some form of mechanical repetition such as a tape loop were employed.

The signal is captured by operation of the REPEAT switch as described in the control section. After a signal is captured, it may be modified by operation of the DOUBLE switch, which speeds up or slows down the repetition by a factor of 2. (If the signal was captured in DOUBLE, putting the DDL in NORMAL speeds it up, if captured in NORMAL, doubling slows it down.) In addition, if the DELAY control is operated, the pitch of the repeated signal may be changed either up or down. The total length of the signal captured is either 320 ms if captured in NORMAL, or 640 ms if captured in DOUBLE. This is long enough for several words, or a short rhythm pattern. By setting the outputs at different delays (or fixing one and varying another), the patterns or words may be caused to overlap, or appear to change sequence. Different psycho-acoustic effects may be obtained by placing the outputs in varying spacial and temporal relationships. Rotating and bouncing effects may be readily obtained.

An interesting effect is that obtained by listening to continuous repetition of a voice type signal. The signal may either consist of words, or word-like sounds. As the repetition continues, the meaning starts to disappear or shift, the words can change into nonsense (or *vice versa*), and other interesting psychological effects may be observed. This manual does not intend to delve into mysticism, but that shouldn't prevent experimentation.

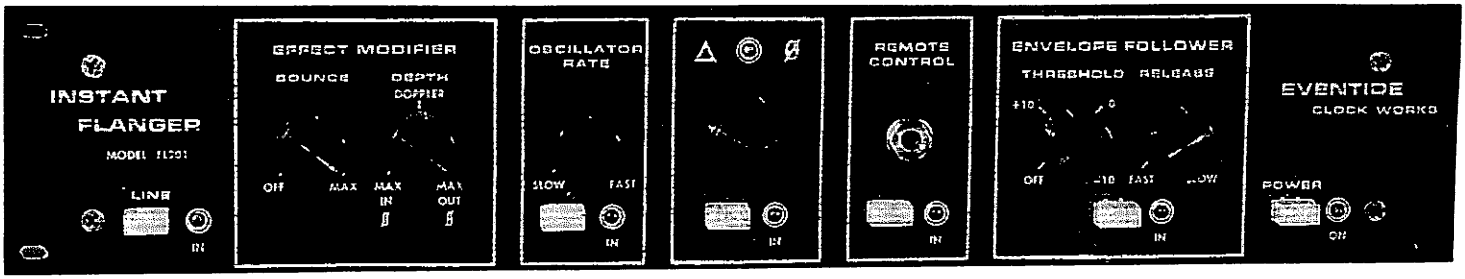
More exotic applications include spectrum analysis for such purposes as voiceprinting and engine signature analysis. The delay line can convert an ordinary swept wave or spectrum analyzer into a quasi-realtime analyzer. Although it isn't by any means the equivalent of a realtime analyzer in terms of processing a large amount of signal rapidly, it can hold a captured signal indefinitely, permitting extremely detailed analysis of the captured portion. The signal is synchronous with the counting of the pointer register, described in the random access memory assembly circuit theory, and various weighting functions can be constructed or various features of the signal excerpted with great precision.

The REPEAT feature can be used to advantage in live performances. The repeat switch can be easily remoted, and control given to the performer by foot switch. Let the live signal come out undelayed or minimally delayed to prevent the performer from being distracted by an excessively delayed return echo. At various points in the performance (usually at the end of phrases or during prolonged vocal harmony notes) activate the REPEAT control and walk away from the microphone. If the performer can juggle, now is a good time to demonstrate it. When he is through, he can step back to the mike and continue.

FLANGING

Eventide manufactures, in addition to the DDL, a rather good INSTANT FLANGER (model FL201). It turns out, however, that the DDL can do a rather fine job of flanging all by itself. All that is necessary is to add the signals from two outputs together and then vary the delay of one up to and past the delay of the other. Because the delays can "slide" past each other, true flanging through 0 delay is realizable. Different effects can be achieved by adding the inputs in-phase and out of phase.

Because the effects created by the Flanger are so similar to those created by the DDL, we felt it would be appropriate to reprint from *Recording Engineer/Producer* an article originally reprinted from our Flanger manual.



PHASING

Since its invention or discovery in the mid 1960's, the special effect known as "PHASING" or "FLANGING" has been one of the most popular additions to the mixer's repertoire. Phasing was introduced to the mass audience in the song "Itchycoo Park" by Small Faces and has been used (yes, and overused) to some extent by virtually every artist since that time. Just in case you've been on an interstellar voyage or in the Phillipine jungles since the 1960's, the phasing effect has been described by various individuals as "a swimming effect," as "a jet plane going through the music," as "a whooshing" sound, as "one of the best ways discovered to cover up mistakes," and as "something that makes you think the music is circling around you." All of these descriptions have merit.

The phasing effect's versatility can be partially explained by the following facts:

1. It affects three of the most important characteristics of a musical signal-pitch, amplitude, and harmonic distribution.
2. It affects signals over a very wide frequency range, and thus applies to virtually every signal source from a bass guitar to a snare drum.
3. It produces dynamic changes in pitch, which is interesting in itself and can be used to cover up mistakes.
4. It can be used to generate a pseudo-stereo signal with interesting characteristics and little effort (pseudo quad too).
5. When used tastefully it can add a hell of a lot of interest to a recording or live performance. (When used without taste it can *still* add a lot of interest. Short of running an entire concert through a phasing device, it's hard to misuse.)

WHAT IS PHASING?
WHAT IS FLANGING?

The terms "PHASING" and "FLANGING" have been used interchangably to describe the effect obtained. In point of electronic fact, there are two substantially different ways of obtaining the effect, and the effect thus obtained is also substantially different. The original effect (used on Itchykoo Park) was allegedly obtained by feeding a signal into two tape recorders, mixing the output, and then placing a drag on one of the reel *flanges* to slow down the machine. Because this method ties up two tape machines, requires 22 patch cords, and is a bit awkward (how many engineers have calibrated fingers?), several manufacturers designed electronic "black boxes" to achieve the effect with greater ease. Typically these devices accept a signal input and produce a phased output, the phasing being controlled by front panel knobs. One manufacturer (Eventide Clock Works) designed a unit specifically for recording studio applications. This unit has several methods of controlling the phasing: in addition to a front panel "$\Delta\Phi$" control, it has provisions for using an internal envelope detector or a variable frequency oscillator, thus phasing automatically either by following the signal amplitude or in a repetitive fashion.

However, (and it's a big however) . . .

HOWEVER these black boxes, for technical reasons, could not generate the same effect as the finger on the flange. And although the black boxes had many advantages which could not (and cannot) be duplicated by the tape flanging method, the effect was not as pronounced or "deep," and thus the tape method continued to be used when a particularly strong effect was desired. To prevent confusion, in the remainder of this article we will refer to PHASING and FLANGING by the following definitions:

PHASING: The effect obtained by using electronic phase-shift networks to generate cancellations in the frequency spectrum of a signal.

FLANGING: The effect obtained by using differential delay to generate cancellations in the frequency spectrum of a signal, regardless of the method used to generate the delay.

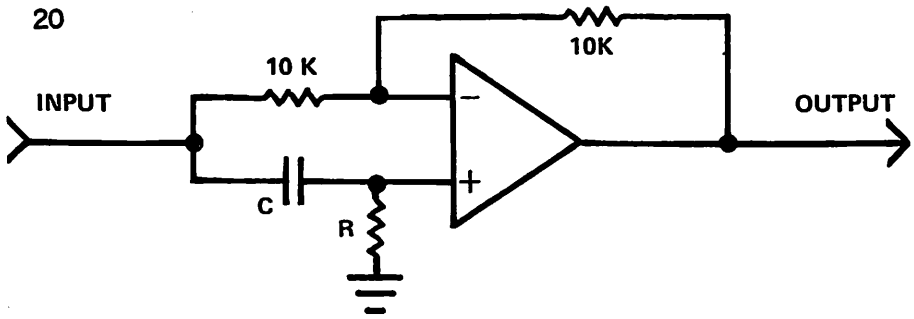
The difference in the sound of the two methods can be well explained by theory, and we proceed to do so below.

PHASING

The basis of the "black box" phasing device is an electronic circuit known as

by RICHARD FACTOR*
Eventide Clockworks, Inc.
New York, N.Y.

* *reproduced from Eventide's Model FL-201 'INSTANT FLANGER' instruction manual.*



the "ALL-PASS NETWORK." As one might assume, this type of network passes signals of all frequencies, but its output phase versus input phase varies as a function of frequency. A representative circuit is diagrammed above.

Since the circuit has a single RC time constant, the maximum phase variation, assuming ideal components, is 180 degrees. In actuality, it can only approach this value since C is limited by stray capacitance and R must not exceed a reasonable value, depending upon the operational amplifier used. The output of the network sounds the same as the input (flat frequency response), but the phase is shifted according to the RC network constants. Thus, by adding the input of the network to the output of the network in a 1:1 ratio, the added signals will be reinforced at frequencies where the phase shift is near 0, and cancelled at frequencies where the phase shift is near 180 degrees. Since our example uses a single network, there will be no complete cancellation. To produce the phasing effect, several such networks are connected in series, and their phase shifts added. This gives rise to such advertising claims as "over 1200 degrees of phase shift!" which is true, impressive, and probably irrelevant. The other requisite for phasing is some method for varying the time constant of the networks over a wide range. In the example shown, varying R over a 400:1 range varies the cancellation frequency over the same amount, causing the phasing to shift from beyond audibility to the mid-bass region. As an added plus, during the period that R is changing, a frequency shift similar to doppler shift is created. This applies to the output of the all-pass network whether or not it is added to the input. Thus it is possible to generate a deep vibrato with no extra circuitry.

The frequency response of 8 all-pass networks is shown graphically for several values of R. The graphs are plotted on identical axes. Since the horizontal axis is logarithmic, the relative spacing of the nulls remains constant, although the absolute spacing in number of Hertz varies as R varies. In observing the graphs, note the following characteristics:

1. Below and above the ranges of the phase shift networks, the output of the system asymptotically approaches 2X the input.
2. The frequency ratio of the nulls is not constant and not harmonically related.
3. The shape of the nulls is sharp, the peaks rounded.
4. The total number of nulls is fixed and dependent upon the number of all-pass networks.
5. At any time the nulls are clustered within one portion of the frequency spectrum.

FLANGING

As we stated earlier, flanging is produced by mixing the output of two tape recorders, one of which is running a little slower than the other. Since the head-to-head distance is fixed, the transit time of the tape from the record head to the play head determines the path delay. Assume that the speed difference between tape machines is such that the differential delay between transit times is equal to 1 millisecond. Since one millisecond is the period of a 1kHz signal, it might be expected that a 1kHz input to the system would result in an additive signal, since the two outputs would add in-phase. On the other hand, a 500Hz input would have a 180 degree phase shift at 1 millisecond delay, and thus would completely cancel. Slightly less obvious is the fact that all signals at odd multiples of 500 Hz will undergo the same cancellation, since, for instance, the phase shift of 1500Hz is 360+180 degrees at 1 millisecond delay. Several graphs are presented showing the frequency response of a signal mixed with its delayed replica. Incidentally, all the graphs show the steady state response. We'll have a few words on transients later. In observing the graphs, note the following characteristics.

1. Below the first null, the output of the system asymptotically approaches 2X the input. There are always nulls at high frequencies.
2. The frequency ratio of the nulls *is* constant and harmonically related.
3. The shape of the nulls is uniform, and similar to the peaks.
4. The number of nulls increases as the delay increases.
5. At long delays, the entire frequency spectrum is substantially modified.

COMPARISON

The consequences of the differences in characteristics are striking. Intuitively, one can feel that the flanging response should have more effect on the music, and in this case intuition is correct.

1. Because there are always nulls at high frequencies, the "jet plane" effect is more pronounced, even when the delay is fairly long.
2. Because the nulls are harmonically related, the effect on the tone of many instruments is more musically interesting. For instance: Assume an instrument is being played with a fundamental frequency of 440Hz. It will have harmonics at 880Hz, 1320Hz, 1760Hz, 2200Hz, etc. At a delay of 1.136 milliseconds, the fundamental and all odd harmonics will be cancelled out, leaving only the even harmonics. If the instrument shifts pitch, its entire tonality will change.
3. There's nothing much that can be said intuitively for advantages of sharp or rounded peaks, and since there's no simple way of comparing them subjectively, let's pass on this one.
4. The number of nulls increases as delay increases, and thus there is an overall broader effect on the input signal. It should be noted, however, that when the nulls are very closely spaced, the effect decreases since there is an averaging between the nulls and the peaks in psychoacoustic realms. As a practical matter, useful flanging occurs in the delay range of 50 microseconds to about 5 milliseconds, and devolves to a doubling effect after about 15 milliseconds.
5. Same comments as above.

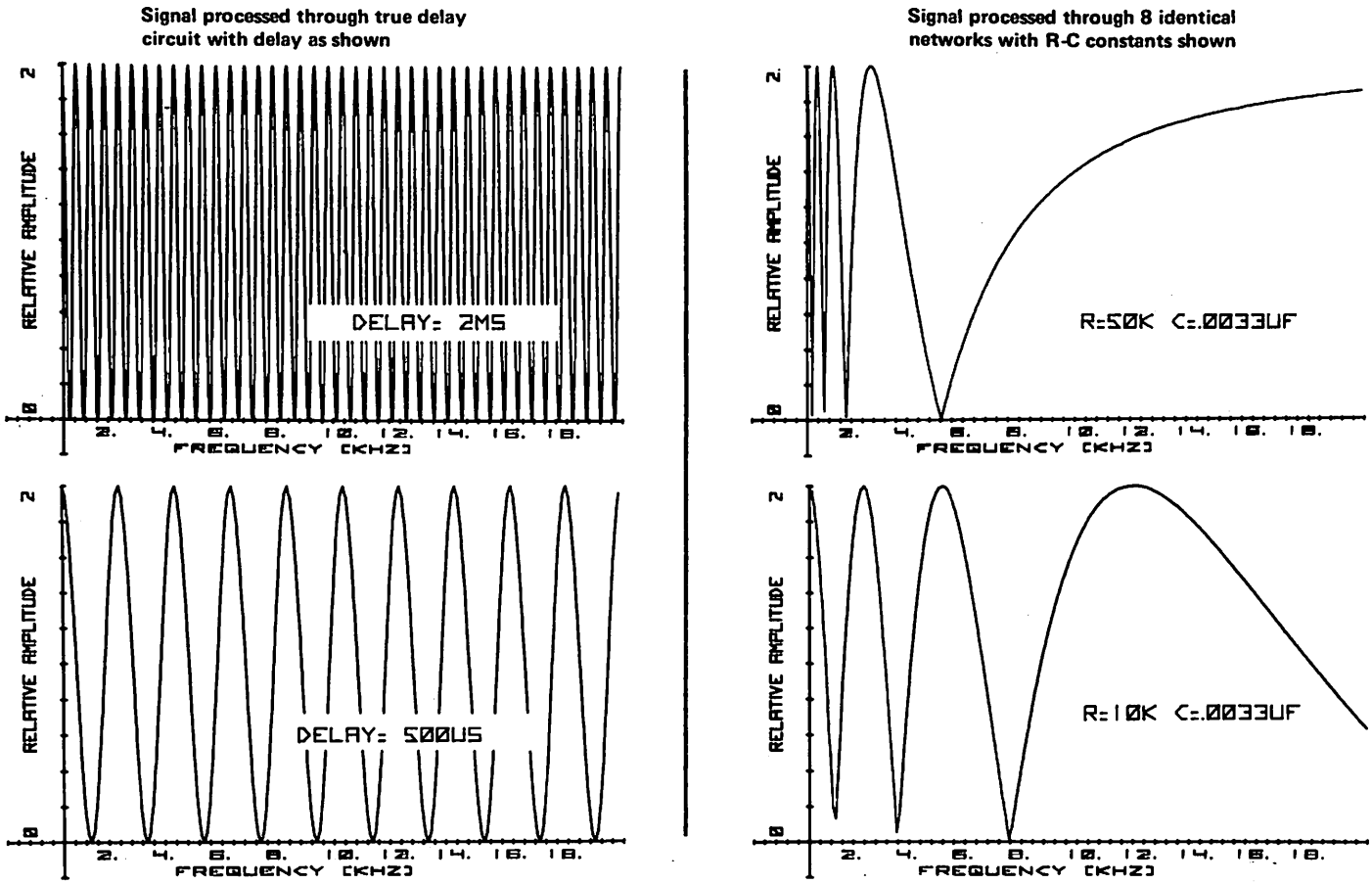
The above comparisons refer only to the steady state behavior of the phasing/flanging systems. In reality, two transient conditions occur (and interact). At issue are the subjective effects when:

1. Material is being phased or flanged while the *time constant or delay of the network is being varied;* and
2. *The input is being changed* while the constants of the network are held fixed.

The results in the first case were alluded to earlier. If a phase shift network has its constants changed, a frequency shift analogous to doppler shift will occur. Since the networks do not affect all frequencies equally, the change will be different for different frequencies. Thus, harmonic ratios will not be preserved during the change. On the other hand, changing the delay in the case of flanging is *precisely* analogous to doppler shift, and frequency shift will take place in the well-known manner. Subjectively, it appears that the *rate* at which the doppler or pseudo-doppler shift takes place is more significant than the type of network that produces it. This is only the result of a few hurried observations and you should feel free to disagree with this conclusion.

Far more interesting is the second case. A phasing network can produce only a limited amount of delay at fre-

PLOT OF FREQUENCY vs. AMPLITUDE OF VARIOUS DELAY TIMES (left) and PHASE NETWORKS (right)
(In each case the graphed response is obtained by the algebraic addition of the input signal to the processed signal.)



quencies in the range that is of musical interest. Transient effects arise because the signal applied to the network input does not affect the final result until it reaches the end of the network. The other branch of signal is direct. For instance, if the delay time were 5 milliseconds and a 1900Hz signal were applied to a flanging network, the output would be a null as indicated in the graph, but, before the null was achieved, 9 complete cycles of the tone would pass through the network, resulting in a cross between a click and a short "beep." Actual musical signals are not nearly so deterministic, and the subjective effects are impossible to describe. That's one of the main reasons why the flanging effect is more pronounced than phasing. In effect, each signal has two characteristics — its steady state and its transient. Although this does not apply particularly to violins, organs, etc., plucked string instruments, and especially drums, take on a whole new aspect when flanged. This effect becomes distinct from the frequency nulling at about 1 millisecond, and increases in importance up to about 5 milliseconds.

In summary, then, the comparison between phasing and flanging comes down to this: Flanging produces a more pronounced effect, primarily because of the extra nulls in the frequency response, and the longer period before transients are nulled out of the final result. It is more difficult to achieve because of the bulky equipment and inconvenient setup and not as controllable.

Reread that last sentence. It's a lie.

FLANGING FOR THE MILLIONS

It seems that achieving short delays in signals has always been difficult. How would you build a delay line variable from, say, near 0 to 5 milliseconds?

If you need a short delay, you can use distributed capacitance and inductance of a coil of wire. As the delay increases, however, the bandwidth suffers. Above a few tens of microseconds, it becomes unusable for high quality audio.

If you need a very short delay, you use a piece of wire and wait for the speed of light to bring you your signal.

If you need a very long delay, you record your signal on tape and play it back later.

If you need a super long delay, you inscribe the data on a silicon wafer and send it into a solar escape orbit.

If you need a few hundred milliseconds of delay, you convert your signal into digital format and store it in shift registers. It will come back unaltered after the desired delay and be converted to analog and reused.

But what about five milliseconds?

The delay is too short to justify the overhead cost of digital technology. A speaker at one end of a tube and a microphone at the other? Fine for fixed delays but try to adapt it for rapid variation! Ultrasonic delay? Suffers from dynamic range problems, and how to vary it? Tape delay? Works, but what a nuisance! Magnetic disc? Costs a fortune and has (ugh) moving parts.

Enough teasing. A new type of semiconductor has been produced in recent years. It is known generically as the "Charge Coupled Device" and popularly as the "Bucket Brigade" delay. Until very recently, the state of development of these devices was such that they were impractical to use for audio. They had insufficient dynamic range and suffered from many undesirable electronic characteristics beyond the scope of this article. As this is written, at least one device is available which is suitable for short delay use in audio with sufficient range, both in delay and amplitude. Earlier devices had been designed primarily for video applications which are more demanding at high frequencies but can get along with 40dB range.

Using these devices to generate delay enables one to build an all-electronic (no moving part) "black box" which produces flanging in a manner precisely analogous, but without the bulk and inconvenience, to the two tape machine-22 patch cord method. An additional benefit is that the delay is controlled electronically instead of mechanically, enabling one to do the same sort of tricks, such as signal or oscillator controlled flanging, as can be done by the common phasing unit.

TUNNELING

The origin of the term is obscure, but if you've ever heard it, the effect itself is quite evident. Consider a tape recorder whose output is connected to its input. Echo, right? And if the gain is too high, rapidly increasing echo, until extreme noise and distortion take over. But if the the gain is j-u-s-t r-i-g-h-t, you get pretty decent repetition, especially if the signal keeps renewing itself from an external source. OK, now, vary the speed of the tape! The pitch of each repetition increases (or decreases). In fact, as long as the tape speed can be kept changing, the pitch will increase or decrease almost without limit. Of course you cannot vary the speed by much more than an order of magnitude, for both electronic and mechanical reasons.

BUT, if you do the same thing with the delay line, you can continuously vary the delay, at a fairly rapid rate. As the delay gets closer to zero, the length of the repetition decreases, and the pitch and frequency of repetition increase.

And, if you vary the delay slowly near 0 delay, you get a very pronounced flanging type effect caused by resonant emphasis of frequencies whose transit time through the delay line are equal to multiples of their wavelength.

And, if you manually vary the rate of delay change, you get a combination of both effects.

And, if you take feedback from 2 or more outputs, you get a complex combination of reverb and flanging which is quite unique.

And, finally, if you experiment, you get things which nobody knows about, because, after all, this is a brand new possibility brought to you by the march of digital technology. Let us know if you find anything interesting for possible future publication.

PITCH CHANGING

As you may have already noticed, rapidly varying the delay creates a change in pitch, precisely analogous to doppler shift (decreasing or increasing source to listener distance). Because of the limited delay change rate of the system, the maximum change, in the DOUBLE mode is about ½octave down, and ¼octave up.

However, the RAM organization of the DDL places no arbitrary limit on the pitch change obtainable. There are three problems present in using the present system for pitch changing:

Limited amount of change available.
Progressive time delay between original and changed signal.
"Data seam" created by rapid change between maximum and minimum delay at zero point.

Fortunately, all these problems are curable, and we have at the time of this writing (JAN. 76) plans to produce a plug-in pitch changing module, to be available in early April 1976, which will allow your 1745M to perform this function quite well indeed.

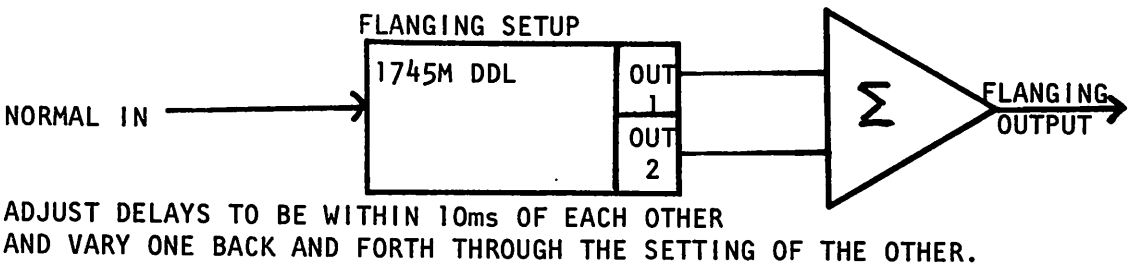
If you have filled in your warranty card, you will automatically be advised of the existence of this module when it becomes available, (and that of other modules including automation-compatible remote control).

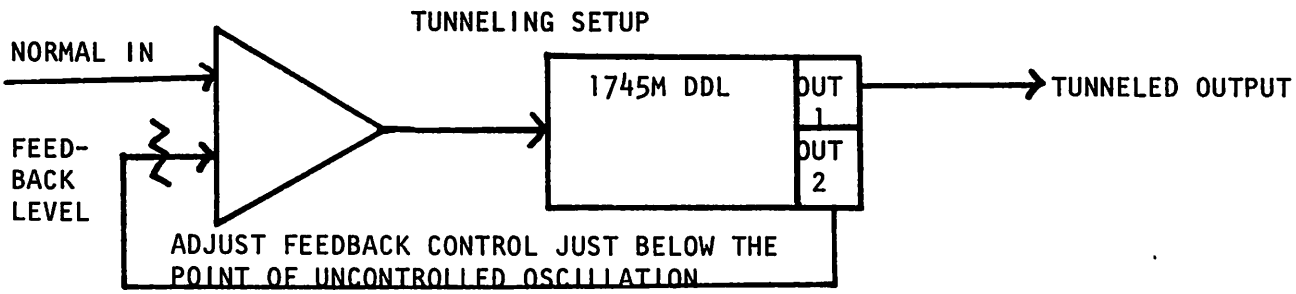
GENERAL WEIRDNESS

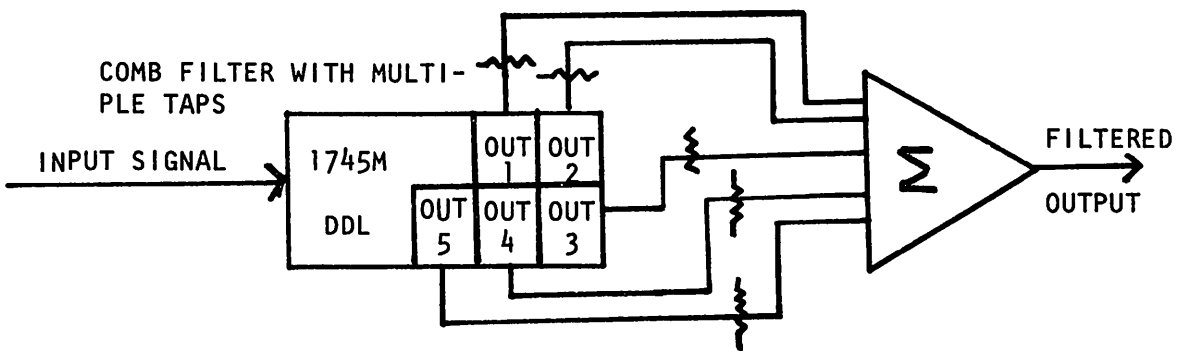
As briefly mentioned in the article *The Digital Delay Line Revisited*, it is possible to read data out of the delay line backwards! We're not quite sure what the applications for this are (other than speech scrambling) but it's so intriguing that we're determined to find out. When we do, we'll send out a note to all our customers, as well as circuit details if applicable.

Solid state echo has long been a dream of the audio engineer, but has remained thus far unrealizable at reasonable cost. The 1745M, with its 5 almost continuously variable outputs, allows one to fulfill at least one criterion of the theoretical work: the requirement for several incommensurate delays. By feeding all the outputs back to the input, varying qualities of echo are obtained, the best being presumable at those delays where each feedback path is a non-integral multiple of the others. The outstanding variability of this system will allow the experimenter to empirically select the best delays for this application.

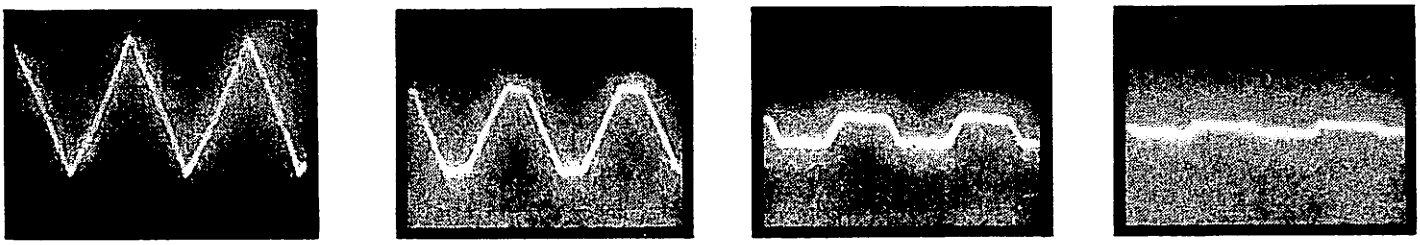
HOW TO DO IT



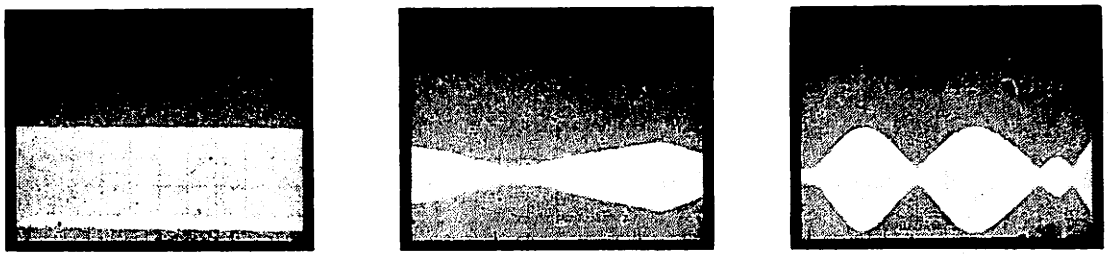




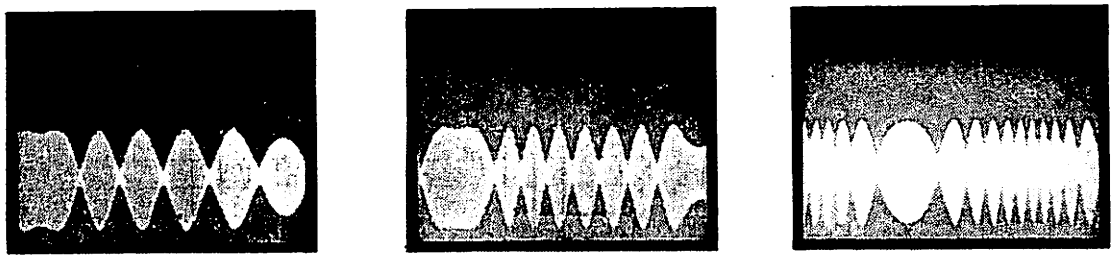
COMB FILTER ILLUSTRATIONS



Triangular wave added to delayed replica of itself. Frequency varied in steps to effect in-phase, partially out-of-phase, and completely out-of-phase additions.



0 ms. **1 ms.** **2 ms.**



9 ms. **16ms.** **40ms.**

Sine wave sweep signal fed into delay line, and the two outputs added algebraically. Number of nulls increases as delay increases, indicating a greater number of out-of-phase conditions. Delay in each case shown under photograph.

SECTION 2
TECHNICAL INFORMATION

The purpose of this section is to enable the technician to understand the 1745M digital audio delay line to a sufficient extent to enable him to:

1: Determine whether it is performing to specification.

2: Identify and repair any possible malfunctions .

To accomplish this, various block and schematic diagrams are presented, as well as descriptions, suggestions, hints, lists, and anything else we feel will be helpful. The final pages of this manual contain reprints of manufacturer's literature about the specific integrated circuits used in the delay line, so that all that should be required for troubleshooting or alignment is electronic knowledge and test equipment.

In a unit as complex as a DDL, it is impossible to cover, or even to think of, everything. For this reason, we strongly encourage you to call the factory if you have any question or problem that cannot be satisfactorily resolved by reference to this manual.

TEST EQUIPMENT

We recommend a certain minimum of test equipment to satisfactorily check out the DDL. Lack of this equipment can turn a simple task into an extremely frustrating one. Analog alignment, absent any true malfunction, requires a minimum of a low distortion signal generator, audio voltmeter, and distortion meter. Frequently all three items are contained in the same package, such as the Sound Technology 1700A Distortion Measurement System or the Radiometer Copenhagen BKF-10.

If there is a digital problem suspected, this equipment should be augmented with a good high frequency oscilloscope, such as the Tektronix 465. For all checkout, a bandwidth of 75MHz is required, and delayed sweep is extremely desirable. A scope with a bandwidth of 10MHz will be adequate if there is no problem with the high frequency oscillator and divider chain.

PERFORMANCE CHECK

The next section details a procedure that can be used to determine if the DDL is functioning properly. In general, it is easy to tell if a suspected problem is analog or digital in nature. Analog problems typically include excessive distortion, poor frequency response, improper levels, and things which just don't sound right. Digital problems usually are indicated by extreme noise, repetitive "glitches" in the output, and very strange looking signals when observed on an oscilloscope.

Of course, if the unit is dead (but still lights up), it could be either, but dead problems are very easy to find. If it is ascertained that a digital problem exists, and you are unfamiliar with digital techniques, it is strongly suggested that the general section on digital troubleshooting be read and understood. It is mandatory that the precautions regarding damage from static charges be adhered to, lest thy warranty be declared *null* and *void*, possibly along with the entire DDL.

PERFORMANCE ASSURANCE

This section is provided to enable the user to determine whether the delay line is operating normally. The left column provides instructions, and the right column describes the indications obtained when the instructions are followed. If the indications are not as described, refer to the troubleshooting suggestions immediately following. If no abnormal indications are obtained, the DDL is functioning normally.

STEP #	ACTION	INDICATION
1	Observe serial plate to determine line voltage. Plug DDL in to proper voltage and turn on power switch.	Front panel numerical readout indicators should become active. No other lights should come on at this time. If readouts cycling, set DELAY knob at center line.
2	Reset all delays, and then place all switches in SET position. Turn DELAY control from end to end.	Delays should at first read 0. As the DELAY control is rotated, all readouts should count up through 319, and back down through 0. All should track perfectly.
3	Momentarily deflect the DOUBLE control up, then down.	2X lamp should become illuminated, and then extinguished.
4	Momentarily deflect the REPEAT control up, then down.	The RPT lamp should become illuminated, and then extinguished.
5	Apply a 1kHz sine wave from a low distortion oscillator to the signal input jack and rotate the GAIN control to maximum. (Input +4dbm)	Observe that all three lamps in the LEVEL box become illuminated. There should be a clipped sine wave present at all output jacks for which an output module is present.
6	Connect a distortion meter to either output and reduce the GAIN control until the output is about +4dbm.	Observe that the red LIM indicator is off, the green NOR and yellow SIG lamps are on. Measure the harmonic distortion percentage. It should be less than .3%.
7	Temporarily decrease the GAIN control until the output level is -6dbm.	Observe that only the yellow SIG indicator remains on.
8	Temporarily decrease the GAIN control to full CCW rotation.	Observe that none of the LEVEL lamps remain on.
9	Raise the GAIN control until the output level is +8dbm. Attach an audio monitor to the outputs, one at a time.	Set the delay to 319 ms. Listen carefully to the output to determine if there is any periodic variation or noise in the output. (Make certain that the DELAY knob is centered.)
10	If possible, repeat step 9 with line voltage at 105VAC (210VAC) and 125VAC (250VAC)	Results should be identical to those in step 9. Be sure to reduce line voltage to nominal.

STEP #	ACTION	INDICATION
11	Set the DDL in the REPEAT mode. Remove the input signal.	There should be a 1kHz signal present at the output. This signal should not decay or change in any way regardless of the number of repetitions. There may or may not be a "click" repeated every 320 milliseconds.
12	Without changing the REPEAT switch, place the DDL in the DOUBLE mode.	There should now be a 500Hz signal present at all outputs, and the "click", if present occurs half as frequently.
13	Return the DDL to all NORMAL modes and reduce the GAIN control until the output level is 0dbm. Vary the input frequency from 30Hz to 16kHz.	Measure the output signal level. It should be constant, ±1db.
14	Adjust the GAIN control until the red LIMit indicator just comes on, with an input frequency of 1kHz. Reduce the input level in 10db steps.	Measure the output level. It should decrease 10db for each 10db decrease in input level. For accurate readings below -60dbm, a selective voltmeter may be required. Decrease should be accurate to 90db below LIM.
15	Apply program material to the DDL input. Adjust GAIN control in accordance with instruction manual. Rapidly vary the delay in each output.	As the delay changes, a smooth pitch change should be evident, both up and down. A deletion or repetition will appear as the delay changes from 0 to 319 or 319 to 0.

Successful completion of the above tests is sufficient to allow one to infer that the delay line is operating properly.

TROUBLESHOOTING

If trouble was encountered during the above procedure, refer to the cause keyed to the step number.

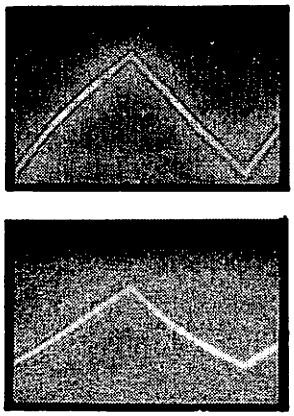
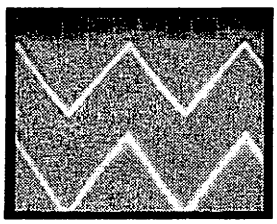
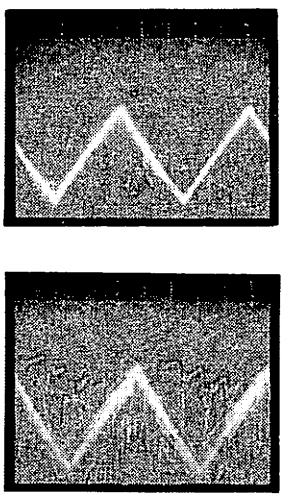
TROUBLE IN STEP#	POSSIBLE CAUSES
1	If no serial plate, inform factory immediately! Check individual power supply voltages. Make sure all boards are plugged in fully. Check internal as well as external fuse.
1 or 2	If one readout goes to zero but not the other, exchange plug-in control boards to isolate defect to plug-in board or output board. If output board, check counters. If plug-in board, check adders and decoder/drivers. If other lights on, check input plug-in board IC's and switches. If neither readout will cycle, check oscillator assembly on input board. If one will not cycle, check counters and plug in board associated with that output.

TROUBLESHOOTING

TROUBLE IN STEP#	POSSIBLE CAUSES
3 or 4	Check switches and IC's on input plug-in board.
5	If lamps work, but only one output present, check defective output board. If lamps work, but no output present, check memory board and circuitry on backplane board. If lamps don't work, check input analog and digital circuitry. If lamps don't work, but output IS present, check input plug-in board.
6	If lamps abnormal but output indication OK, check level detecting circuitry on input board. If everything OK but distortion is high, look at output signal with oscilloscope. If digital problem, check for defective memory or conversion circuitry. If analog problem, refer to alignment procedure before proceeding.
7	Check level detecting circuitry.
8	Check level detecting circuitry and adjustment of offset trimpot.
9	Periodic noise almost certainly indicates a defective memory chip. Locate and replace as described in digital troubleshooting suggestions.
10	If problem, such as hum or erratic operation at low line voltage, check bridge rectifiers for open diode. (Look at unregulated DC on filter capacitors. If ripple is 50 or 60 Hz, it is almost certainly a defective rectifier.) If 120Hz, check for bad or leaky capacitor, or defective regulator IC. If problem at high line, check for defective regulator.
11	If REPEAT function doesn't work at all, check that WRITE pulses are being inhibited at the memory chips. If function works but signal decay or noise buildup is evident, check all cables for loose connections, and check environment for extremely strong RFI or line transients.
12	Check that input plug-in board contacts are clean, and that inhibit flip-flop is functioning properly.
13	If slightly off at high end, touch up adjustment of filter peaking control. If seriously off at high end, look for defects in low-pass filters on input and output boards. If seriously off at low end, look for defects in compressor and expander cards.
14	If linearity is off at top of dynamic range, suspect defective compressor or expander cards. If both outputs don't track, problem is probably one of the outputs. If linearity is off at bottom of dynamic range, suspect less significant bits of memory or A/D or D/A converters.
15	Check oscillator for instability. Trigger scope on delay change oscillator and observe sampling pulses. As the oscillator rate is increased, the number of sampling pulses between delay change pulses should decrease in steps. If there is substantial jitter or lack of synchronization, check related circuitry.

TROUBLE INDICATIONS

If the delay line is *almost* functioning properly, waveforms such as these below may be obtained. Possible causes for the abnormality are indicated next to the scope photos.

SYMPTOM	OUTPUT SIGNAL	POSSIBLE CAUSE
Excessive distortion (triangular wave input)		Misalignment of distortion trim adjustments or defect in current sink on input board. If all outputs show an identical problem, the problem is on the input board. If only one output has distortion, problem is with that output. The photographs show serious misalignment. Slight alignment errors will not be visible but will show up with distortion measuring equipment.
Noisy signal, "frying sound", "granularity" Note difference in bottom trace.		One or more of the less significant bits missing from the output. Indicates possible bad memory IC if both outputs bad, or defective output latch or D/A if one output bad.
Extremely noisy: pops, crackles, output has "glitches"		If 60 or 120 Hz component, probable power supply problem, or low line voltage. If glitches appear repetitively, probable defective high order bit in memory, or defect in input A/D converter or timing. If glitches seem temperature dependent, also check alignment of output boards.

ALIGNMENT INSTRUCTIONS

The delay line is aligned at the factory, and the alignment is sufficiently stable so that periodic readjustment should not be required. If it is desired to align the unit, either for reassurance or because some component or assembly has been changed, the following procedures should be followed. The analog adjustments will require a low distortion signal generator and distortion meter; the digital adjustments will require an oscilloscope with a calibrated time base capable of measuring time to about 50 nanosecond accuracy on a 3-10 microsecond scale.

The following assemblies have no adjustments which need be performed:

Mother Board
Memory Board
Input plug-in Board

The output plug-in board doesn't require alignment. However, the screwdriver adjust LEVEL control should be centered before beginning output board alignment.

INPUT BOARD ALIGNMENT

1: Remove all output boards
2: Refer to schematic diagram for control locations on Compressor card.
3: Turn GAIN control fully clockwise. Apply 1kHz, -10dbm input signal to DDL.
4: Attach distortion meter probe to pin 12 of compressor module.
5: Adjust COMP LEVEL control to obtain 3V RMS at this point.
6: Adjust VCA SYM control to obtain null in second harmonic, or null in distortion.
7: Reduce input frequency to 100Hz. Adjust RMS SYM control for null in distortion. IMPORTANT NOTE: Both of the above controls vary the output level in addition to nulling the distortion. Be sure that a true distortion null is obtained.
8: Repeat steps 5,6, and 7 if significant adjustment was made in any step.
9: Remove input signal and turn GAIN control fully CCW. Adjust the OFFSET control in either direction until the yellow SIG light just goes off, if on, or comes on if previously off. When the on/off point is established, turn the control 1 turn in the direction necessary to extinguish the lamp.
10: The HF PEAK trimpot adjusts the frequency response at the high end. Since it must be varied with an OUTPUT board present, defer adjustment temporarily.

OUTPUT BOARD ALIGNMENT

1: Insert the board to be aligned in the slot immediately next to the input board. Digital alignment
   A: Trigger the oscilloscope on the T5 test point on the input board, and adjust the display for a time base of about 500ns per division. The vertical scale should be 5V per division (500mV/division if a 10X probe is used).
   B: Observe pin 6 of IC-15 on the oscilloscope, and make sure that the beginning and end of the pulse are clearly visible and stable. Adjust BE (Bus Enable) so that the length of this pulse is 2.6 microseconds.
   C: Observe pin 10 of IC-15 on the oscilloscope. Adjust CED (Chip Enable Delay) so that the length of the pulse is 2.0 microseconds.
   D: Observe pin 5 of IC16. Adjust CE (Chip Enable) so that the length of the pulse is 450 nanoseconds.
2: Apply a 1kHz input signal and adjust the GAIN control so that the red LIM indicator is on the verge of becoming illuminated. Check the DAC output test point to confirm that a sine wave is present. Level should be approximately 3VRMS.
3: Adjust the EXP LEVEL control until the level as measured at the 150ohm output

is 7VRMS.

4: Adjust VCA sym control to obtain null in second harmonic, or null in distortion.

5: Reduce input frequency to 100Hz. Adjust RMS SYM control for null in distortion. IMPORTANT NOTE: Both of the above controls vary the output level in addition to nulling the distortion. Be sure that a true distortion null is obtained.

6: Repeat steps 3,4, and 5 if any significant adjustment was made in any of those steps.

This completes the alignment of the output board. Repeat the procedure for each output board in the system.

INPUT BOARD FILTER ALIGNMENT

Apply a 1 kHz input signal and adjust the GAIN control until the output level is -4dbm. Change the input frequency to 15kHz and adjust the peaking control until the output level is -4dbm.

Do a frequency response run and confirm that response is within specification. If there is an excessive peak at the high frequency end, readjust the peaking control 1 db at a time until the overall response is satisfactory.

MECHANICAL ALIGNMENT

If the DELAY knob has been removed for any reason, it should be replaced carefully to be certain that the physical center corresponds to the electrical center. The easiest way to do this is to apply a high frequency (about 5KHz) to the input and monitor the output. As the delay is varied slowly, a series of tiny clicks may be heard. As the DELAY control is rotated toward the center, the rate will decrease, stop and then increase. Rotate the control until the shaft is centered in the stopped position. Replace the knob so that the pointer is precisely centered over the divider.

This completes the alignment of the 1745M.

THEORY OF OPERATION

The purpose of this sub-section is to describe in a fairly specific manner the method by which the delay line operates. The various circuit sub-groups are dealt with individually, with reference to what each one does, and how it does it. To make this section of a manageable length, we assume that the reader is familiar with the individual integrated circuit "building blocks", and so will describe the IC's place in the scheme of things rather than the operation of the IC itself. Pin connections and brief descriptions of the IC's will be found at the end of this manual.

There are 7 different printed circuit assemblies which contain the circuitry of the DDL. They are:

DESIGNATION	ASSEMBLY NUMBER	TOTAL: STANDARD	OPTION 03
BACK PLANE "MOTHER BOARD"	M780	1	1
RANDOM ACCESS MEMORY BOARD	5480	1	1
INPUT FILTER AND TIMING BOARD	M691	1	1
INPUT BOARD CONTROL ASSEMBLY	M592	1	1
OUTPUT D/A AND CONTROL REGISTER BOARD	M694	2	3
OUTPUT BOARD READOUT AND CONTROL ASS'Y	M594	2	3
COMPRESSOR/EXPANDER ASSEMBLY	303A	3	4

Up to a total of 3 extra outputs (option 03) may be ordered. Each consists of 1 ea. assembly type M694, M594, 303A

All of the circuitry and all of the controls of the DDL are on these assemblies, with the following exceptions:

5 Output (male) XL connectors and 1 Input (female) XL connector are mounted on the rear chassis panel and connected to the mother board by a 14 conductor cable.

The +5 and +15 volt integrated regulators are mounted on the left chassis panel and are connected to the mother board by a 6 conductor cable.

The AC input connector is mounted on the rear chassis panel and is connected to the mother board by a 3 conductor cable, which is also used to select the supply voltage.

The AC POWER ON/OFF SWITCH and external fuseholder are mounted on the front chassis panel and are permanently wired to the mother board.

The mother board is connected to the random access memory board by 3 16 conductor jumper cables and a 6 conductor jumper cable. All of these cables correspond pin-for-pin on each end, so that a signal appearing on, say pin 3 on socket A on the mother board also appears on pin 3 of the corresponding socket on the RAM board.

Other than that listed above, there are NO CABLES, and NO HAND or HARNESS wiring in the delay line. All printed circuit assemblies plug together. Structural rigidity is provided by the chassis and panel assembly, all components of which except for the rear panel are employed to keep the PC boards in their proper relationship.

The following descriptions will be easier to follow when used in conjunction with the block and schematic diagrams.

CIRCUIT DESCRIPTION: BACK PLANE "MOTHER BOARD" ASSEMBLY M780

This assembly contains components and printed wiring to perform the following system functions:

1: Supply regulated DC voltage to the remaining circuitry.
2: Interconnect the various input, output, and memory modules.
3: Provide voltage level translation between the input card and the memory and output cards.
4: Provide physical space and support for optional output balancing transformers.
5: Accept the chip enable signals from the various output modules and combine them.

1: The power supply generates the following voltages:
A: +15 volts for the analog and CMOS circuitry
B: +12 volts for the random access memory chips and memory board.
C: +5 volts for the TTL logic on the input board and readouts on the output boards.
D: -6 volts V_{bb} supply for the random access memory chips.
E: -15 volts for the analog circuitry.

The +15, +5, and -15 volts are in each case generated by a standard power transformer driving a full-wave bridge rectifier, capacitor input filter, and an IC regulator chip. Current capacity at +5 and +15 is 1 amp. Current capacity at -15 is 250mA, limited by the heat sinking capability of the P.C. board

The +12 volts is generated by connecting three silicon diodes in series with the +15 volt supply and loading the output of these diodes by the essentially constant drain of the memory board.

The -6 volts is generated by a resistive voltage divider from the -15 volt supply to a zener diode. Current drain from this supply is typically less than 1 mA.

2: The board and its associated 22pin edge connector sockets serves as a physical support for the other circuit boards. (Note this board is 1.5 times as thick as the other cards, and is edge supported at four places each on the top and bottom of the chassis.) The various address and data busses are parallelled to each socket, and to the sockets for the jumper cables that go to the memory card.

3: The CMOS circuitry on the input card operates at 5 volts so that it may interface with the high speed schottky TTL circuitry. The balance of the system CMOS circuitry operates at +12 or +15 volts so that it may be fast in its own right. An IC buffer type 74C902, and its associated RC networks increase the output voltages as required.

4: If the 1745M is ordered with any quantity of option 05, the appropriate transformers are mounted on the mother board. If these transformers are not supplied, the transformer mounting holes are jumpered to provide signal continuity.

5: Each output module generates a chip enable circuit sequentially. An eight input gate 74C30 combines and inverts these signals and passes them to the memory.

CIRCUIT DESCRIPTION: RANDOM ACCESS MEMORY BOARD ASSEMBLY 5480

This assembly contains components and printed wiring to perform the following system functions:

1: Provide a sufficient number of bits of memory to store a digital representation of the input analog signal for 320 milliseconds (160 milliseconds option 02).

2: Provide a "pointer" or "base address" register to keep track of the location of the most recently entered data.
3: Provide a binary and binary-coded-decimal (BCD) high speed adder to add the desired delay to the current location.
4: Provide a BCD to binary converter to convert the mixed system to a usable address for the memory chips.
5: Provide decoding and driving circuitry to interface the memory chips to the address and chip enable logic of the remainder of the system.

1: The random access memory comprises 40 integrated circuits (20, option 02), each of which is capable of storing 1 bit of data in each of 4096 address locations. The memory organization is "10 by 16384", or "10 by 16K". Each data word (sample) consists of 10 bits of parallel data. These 10 bits are written and read simultaneously from the active group of memories. The active group is determined by decoding the two most significant bits of address data from the adder (3) into one of four lines, and the chip select lines of that group are then activated. .

The memory chips themselves are of the "dynamic" type, that is they require a "refresh" operation at each of their low-order address locations every 2 milliseconds. Because the data are written into each location sequentially, the refresh requirement is automatically satisfied without further circuitry. Note that this is true even in the repeat mode when no data are being written. As long as each address is activated, that address is refreshed, regardless of the write, chip select, or data lines.

In order to assure ready availability of these IC's, we have performed tests on those of many manufacturers. As there are 40 identical chips in the DDL, failure from a defective memory is one of the most likely possible defects. If it becomes necessary to replace one, we can recommend replacement according to the following table:

Manufacturer	Part Number	Acceptability
National Semiconductor	MM5280D-5	GOOD
Texas Instruments	TMS4060	GOOD
Intel	2107A	GOOD
Intel	2107B	GOOD
Western Digital	RM1701H	GOOD
AMI	S4021	GOOD
AMD	AM9060	INQUIRE
Intersil	IM7507	NOT ACCEPTABLE

In general, any of the memory grades (access time) will be usable. If a part does not appear in this table, call the factory before trying to use it.

The individual memory chips may be located on the board and schematic diagram by a coordinate system, the row and column designations being etched on the board.

2: The pointer register is decremented every time a sample is written into the memory array. Thus this register points to the current data address. Adding a number to the number in this register gives the address of data that number of samples earlier. As each sample is separated from the previous one by 20 microseconds, the delay may be incremented in 20 μs steps by adding to the pointer address. The register consists of 3 BCD counters and one binary counter, IC's A1, B1, C1, and D1. The decrement pulses are generated by the timing card, one pulse per sample normally, and one every two samples in DOUBLE. The alternate decrement results in data being overwritten at the same address, effectively destroying alternate samples.

3: The BCD/Binary adder consists of IC's A2, B2, C2, (BCD) and D2 (binary). These IC's accept one set of inputs from the pointer register previously described, and another set of inputs from the delay selection bus. The output is the arithmetic sum of both numbers, which represents the address of the data that wereinput a certain number of samples earlier. The delay selection bus is controlled by the various output modules and may present several different addresses during each sample interval. To assure that data arewritten into the pointer register location, a resistor network (B3) loads the bus so that all data lines are at logical zero at write time.

4: The BCD to Binary converter consists of 4 bit binary adders B4, A4, D3, C4, and D4. The 12 bits of BCD data representing addresses 0 through 999 are applied with the proper weight to various inputs of the adders. For instance, IC2-13 represents a decimal 20, so it is connected to two terminals on A4, equal to binary 4 (2^2) and binary 16 (2^4). When this line is at logical 1, the output of the adder is the binary equivalent of the decimal input. The OR gate A3 is used to combine outputs for which there would otherwise be insufficient inputs on the adders.

The output of the converter gives the binary equivalent of the decimal inputs, compacted into 10 lines, which are the addresses AØ through A9 applied to all chips of the memory array.

The output of D2 is already in binary format and the two least significant bits from this adder are applied to the memory array addresses A1Ø and A11. These are all the address lines that are directly available. The most significant two bits from the binary adder go to:

5: The decoding and driving circuitry. IC 23 is a decimal decoder, the first four outputs of which are enabled. The two binary lines are decoded into four possible states, each of which enables the chip select inputs of one of the memory groups. This is in effect external address decoding, since the RAM chips are limited as to the number of pins available.

IC 24 ANDs the write enable line from the timing card with the various chip select lines to prevent writing into the wrong locations. IC26 AND's the chip enable line from the timing card with the outputs from IC25, which in turn OR's the chip select lines with the refresh enable line from the timing board. The refresh enable signal assures that at least one chip enable signal is applied to each memory chip even when that chip is not selected. If this were not done, the refresh requirements would not be met. If CE were enabled all the time, the power dissipation of the memory array would increase substantially.

As the memory address and CE inputs are connected in parallel, they can present capacitive loads to the CMOS IC drivers. To increase the speed of the circuits, four address buffers are employed, IC 21, 22, 28 and 29. These chips are CMOS, but are capable of higher current drive than standard circuits. Each output drives 20 address lines in parallel.

To drive the CE lines, complementary transistor buffers are driven directly from another CMOS buffer chip, IC 27.

CIRCUIT DESCRIPTION INPUT FILTER AND TIMING BOARD ASSEMBLY M691

This assembly contains components and printed wiring to perform the following system functions:

1: Convert a balanced audio input signal to an unbalanced-to-ground signal.
2: Compress the audio signal by a 2:1 ratio.
3: Low-pass filter the audio signal to remove components which could cause aliasing.
4: Convert instantaneous signal levels to a digital pulse width.
5: Convert the pulse width to a data signal which may be stored in memory.
6: Generate the timing and synchronization signals necessary for system operation.
7: Decode the various digital signals to produce front panel LEVEL indications.
8: Generate variable speed pulses to control the output board delay registers.

1: IC1 and IC2 are voltage follower operational amplifiers which isolate and buffer the balanced input signal. The two 4.7K input resistors and .001µF capacitors provide a measure of protection from overvoltage, and some high frequency rolloff. IC3 differentially amplifies the still balanced signal and converts it to a single-ended source. The transformer and 620 ohm resistor are provided optionally if transformer isolation and/or 600 ohm input is required.

2: The compressor module consists of two sections, a level detector, and a variable gain stage. The level detector measures the output level and provides a DC feedback signal to control the variable gain stage. The gain control constants are such that each 10db increase in input produces a 5db increases in output. This card is identical in construction and component values to the expander card on the output modules. They differ only in connection of pre and de-emphasis, and mode of operation (expand or compress). As their characteristics are complementary, their operation is transparent as far as the input and output signals are concerned. Their wide range is obtained by taking advantage of the logarithmic characteristics of junction transistors which produce a linear decibel relationship between input and output.

3: IC 4 and IC 5 and associated passive components are each 2 pole active filters which combine with the rolloff of the input RC sections to produce severe attenuation of high frequencies above 16kHz. The peaking trim resistor adjusts the high Q filter section for optimum response.

4: The audio output from the filter is applied to a MOSFET transistor operated in the switching mode. When this transistor is ON, the signal is applied to ~~the .0027µF~~ .0037µF capacitor C8. When the transistor is OFF, this capacitor is discharged linearly by a current sink formed by the 2N3391 transistor and associated reference voltage diodes. The discharge time is directly proportional to the voltage on the capacitor at the time the transistor is turned off. A DC offset is applied to the signal at the input to the filter so that the usable signal is restricted to a positive range of 0 to about 6volts. IC3 ~~IC6~~ is a high speed comparator which is referenced to ground. When the potential on the capacitor crosses 0 volts, the comparator shuts off. Thus, the comparator output pulse width is proportional to the signal level on the capacitor.

5: The output of the comparator is gated with a timing pulse by IC14, and this signal is applied to the enabling inputs of a high speed TTL counter operating at 64MHz, IC10. The second section of IC10 takes the 32MHz output from this counter and divides it to 16MHz, and further applies it to IC12 and IC11, two four bit counters. The capacity of these counters is 1024 counts, although they are limited to slightly less by preventing premature turn-on (see timing diagram). After the counters are turned off, they contain a binary number indicative of the input level for that sample. This number is applied through 3-state buffers IC8 and IC9 to the memory board. When the data are loaded in memory, the counters are reset in preparation for the next sample.

6: IC15 is the master timing oscillator for the DDL. It employs a 64MHz, third

overtone quartz crystal for frequency selection and an ECL line driver integrated circuit operating in a linear mode for feedback, amplification and buffering. The output of the ECL oscillator is applied to a pair of high-speed PNP transistors in a differential configuration to convert the signal to TTL levels, and a high speed TTL gate for further buffering. This signal is applied to IC13, which reduces the signal to 16MHz, and thence to 4 bit counter IC17, which reduces it to 1 MHz, IC 18, 1 section of a CMOS flip flop, which reduces it to 500kHz, and IC16, a CMOS divider/decoder which produces 10 different signals, TØ through T9, every 20 microseconds, which is the basic sampling interval. These intervals are decoded, along with some higher speed pulses, by various portions of IC's 19, 20, and 21 to produce the memory control signals "write enable","chip enable", and "refresh enable", as well as control signals for the counter (5, above). For the time relationship of these signals, refer to the timing diagram.

IC18 (pins 1,2,3,13,13,14) controls the DOUBLE mode. When this FF is enabled, it is toggled by T5, and used to inhibit the output of IC19 12 or 8 on alternate samples. This prevents the memory pointer register from decrementing, resulting in different data being written into the same address, thus destroying alternate samples.

IC20 pin 13 controls the REPEAT mode. When this signal is brought to logic 0, the output of IC20, pin 12 is held high, preventing decoded write enable signals from reaching the memory. This freezes the memory contents.

7: Signals that control the front panel LEVEL indicator lamps are generated by one section of IC23 and IC25, which are J-K flip flops. These FF's are reset on each sampling interval, and then set if the A/D counter reaches a high enough count. Because of the DC offset, all three FF's normally become set. If a small signal is present, the sig PRESent FF will sometimes not be set. If a ¼scale signal is present, the NOR FF will sometimes not be set. If a full scale signal is present, the LIM FF will sometimes not be set. When any of the FF's is not set during a sampling interval, a 0 is presented to the appropriate terminal of monostable multivibrators IC22 and 24. This 0, in conjunction with inverted timing pulse T9 triggers the monostable, which stretches the pulse into an interval long enough to provide a visible indication, and sends the pulse to the input control plug-in board.

8: IC 26 and the five associated transistors form a wide range current controlled oscillator which works as follows: The three upper NPN transistors and 1N914 steering diodes form a ground-referenced "current mirror" circuit, which sinks current from the .056 capacitor, normally charged to +15 volts through the 22M resistor in parallel. If the input current is negative, the upper transistor sinks current; if positive, the bottom two transistors invert the current and sink it. This current linearly charges the capacitor to the CMOS threshold of the dual D flip flop. The FF is continuously clocked by the sampling oscillator, whose voltage is increased to 15 volts by the lower NPN transistor.

When the capacitor voltage reaches the CMOS threshold, the following sequence takes place: Pin 5 goes low, thus placing a 0 on the D input of the following stage. On the next clock pulse, this section goes low, resetting the first section and causing the PNP transistor across the capacitor to conduct and discharge the capacitor. Resetting the first section causes the D input on the second section to go high, and on the next clock pulse the second section is reset.

The result of all this is that the oscillator will produce pulses, synchronized to T9, at a rate proportional to the capacitor charging current, which can be varied over an extremely large range by varying the voltage at the input to the current

mirror. The 22M resistor provides a small "deadband" by assuring that the capacitor will not charge with extremely small values of input current. The maximum charging current is governed by the two 4.7K resistors going to the control pot on the plug-in board.

IC 27 is a comparator which determines whether the control voltage is above or below zero. If above, pin 6 goes positive and asserts the UP/DOWN line. If the comparator goes negative, the diode and resistor to ground on the output prevent negative voltages on this line.

CIRCUIT DESCRIPTION: INPUT BOARD CONTROL ASSEMBLY ASSEMBLY M592

This assembly contains the various controls necessary to operate and observe the functions of the INPUT assembly described above.

This card contains the following:

1: The DOUBLE switch, and latch, which consists of one section of a CMOS AND gate. The output of the latch is applied to IC18 pin 2 on the INPUT BOARD, and to one section of a CMOS buffer which drives the 2X led on the plug-in board.
2: The REPEAT switch, and latch, whose output is applied to IC20 pin 13 on the INPUT board, and to one section of a CMOS buffer which drives the RPT LED.
3: 3 additional CMOS buffers and LED's which indicate LEVEL.
4: A GAIN control which varies the signal level going into the compressor module.
5: The DELAY control, which varies the current into the oscillator (8, above).

CIRCUIT DESCRIPTION: OUTPUT D/A AND CONTROL REGISTER BOARD ASSEMBLY M694

This assembly contains components and printed wiring to perform the following system functions.

1: Store desired delay information for output in question.
2: Provide for placing this information on the delay selection bus at the proper time.
3: Accept digital data words from the random access memory and convert them to analog format.
4: Low-pass filter the resulting analog signal.
5: Expand the analog signal to restore the dynamic range to that of the original input signal.
6: Perform sequential timing functions to accept and transmit triggering signals.

1: The delay storage register consists of 3 BCD counters, IC's 1-3, and a binary counter, IC-4. These counters receive pulses from the input board oscillator through IC8, which steers them according to the sense of the UP/DOWN line. The preset inputs of the counters are each connected to their respective bit on the delay select bus and may be set to a given delay in parallel. This feature is optionally available for use with remote control.

2: The outputs of the counters are placed on the bus through IC5, 6, and 7, which are CMOS tri-state buffers activated by the timing circuitry described below. The timing assures that only one group of signals is active at a given time.

3: Two six bit latches, IC9 and IC10, are connected to the read data bus, and are strobed by the timing described below. At the time of strobing, the data on the inputs of the latches corresponds to the delay selected by the register, and these data are transferred to the outputs of the latches, and into a monolithic ladder type

digital to analog converter. This converter has a current output, which is converted to a voltage output by IC12, which also acts as an RC low-pass filter.

4: IC 13 is a two pole active filter which further restricts the frequency response of the output signal, and removes most of the high frequency clock component of the output signal.

5: The expander module operates in a manner analogous to that of the compressor module on the INPUT board. The external wiring is changed so that the level detector accepts its input from the input of the gain control section, and the control polarity is reversed so that the gain is increased as the input level increases.

6: The timing circuit consists of three monostable multivibrators which act as follows.

BE (bus enable) generates a 2.6 microsecond pulse, which is triggered by the conclusion of a memory write operation if the output is first in line after the input, or by the conclusion of the previous bus enable if second or further in line. The trailing edge of this pulse also strobes the data latch in (3) above. While this mono is active, the tri-state buffers in (2) above are also activated and the delay register outputs are on the bus.

CED (chip enable delay) is triggered simultaneously with BE, and produces a 2.0 microsecond pulse.

The conclusion of the CED pulse triggers CE (chip enable), which generates a 450 nanosecond pulse.

These pulses control the memory as follows: BE places delay register data on the bus, which areadded to pointer register data to address the memory. CED provides a time delay during which the various adders on the memory board compute and transfer the address to the RAM chip, after which CE strobes the address in the memory chips and after a short delay (determined by the memory chip), present the read data on their individual output lines. After the data is latched, the bus is released and the next output is triggered. Five slots are available, and each slot, if filled requires about 2.7 microseconds of bus time. Thus, the bus will be free in a maximum of 13.5 microseconds, allowing plenty of time for the address lines to go to zero and to address the memories to the pointer register location in preparation for a new sample.

CIRCUIT DESCRIPTION: OUTPUT BOARD READOUT AND CONTROL ASSEMBLY ASSEMBLY M594.

This assembly operates in conjunction with its associated OUTPUT board to perform the following functions:

1: Read out (to the nearest millisecond) the data contained in the delay register.
2: Control the pulses used to set the register, and reset the register
3: Provide a narrow range level control for its output.

1: The readout consists of 3 seven-segment light emitting diode displays, each driven by a TTL low power decoder driver. These drivers (IC1, 2, 3) require a BCD input. The register provides an unusual format output, lines indicating 1, 2, 4, 8, 16, 20, 40, 80, and 160 milliseconds, which are not entirely compatible with the decoder drivers.

IC5 is a BCD adder which accepts the first 5 input lines and, by connecting each line to two equal-weighted inputs, effectively doubles the number. The first line goes to the carry input and adds 1 to the sum. The second adds 2, the third adds 4, the fourth adds 8, and the fifth adds 16. Since the output format is BCD, any sum greater than 9 generates a carry, which is applied to the least significant input on the second digit. Although the input lines are binary weighted, their sum is prevented from

exceeding decimal 19, and so no illegal states are generated.

IC4 is a ROM programmed to convert binary to decimal. Its truth table is such that for any binary input from 0 through 63 will produce a BCD output which corresponds. The least significant bit is identical in BCD and binary and so bypasses the ROM and the remaining lines, since they represent decimal 10 times the binary input, are scaled over by one decimal digit to read 0 through 639. The input line corresponding to 320 is permanently grounded, as this exceeds the unit's memory capacity.

2: The SET/ZERO switch is connected to IC8 on the output board and enables or inhibits passage of the delay change pulses. Putting the switch in the momentary ZERO position brings pin C high, which resets the register. (The capacitor from pin C on the output board to +15V performs this function automatically whenever power is applied.)

3: The level control is connected between +15 and ground, and it's wiper arm goes through a resistor to a bias point on the expander module. This control has about a 6db effect on the output level, and, if desired, may be increased in range by lowering the series resistor.

This completes the circuit description.

MECHANICAL ASSEMBLY AND ACCESS

The DDL is held together by many screws, nuts, brackets, and captive fasteners. Following the procedures detailed below will enable one to perform the desired changes or service operations with a minimum of vindictive invective.

ALIGNMENT: All adjustments with the exception of high frequency peaking and DC offset may be reached by removing the top cover.
The high frequency peaking and DC offset controls can be reached by removing the cover in standard units. If the DDL has three or more outputs, board clearance will make adjusting the controls awkard, but not impossible. Adjustment will be easier from the bottom in this case.

IMPORTANT: Never remove the top and bottom cover simultaneously unless it is desired to remove the entire electronic assembly from the chassis.

FOOT REMOVAL For rack mounting, remove the bottom cover and then remove the feet. Do not leave loose hardware in chassis.

OUTPUT CARD REMOVAL

1: Remove top cover.
2: Remove 4 screws holding panel to chassis.
3: The input/output modules and panel may now be removed from the backplane by pulling forward to remove them from their sockets.
4: Remove from front panel by removing bottom screw from panel side and top screw from bracket attached to board.
5: Push output card away from readout card and lift out.

INPUT CARD REMOVAL Follow procedure above

INPUT CONTROL CARD REMOVAL Follow card removal procedure, then remove the two screws holding the input control card sub-panel. Remove all knobs and switch nuts, and remove card from rear.

READOUT CARD REMOVAL This card may be removed without removing output card in delay lines with 3 or fewer outputs. Remove screws holding sub-panel and push readout card away from socket. Then, remove switch nut and remove card from rear of panel.

RE-ASSEMBLY The easiest way to return the cards is to place the DDL on its rear, front panel up. Then, all cards may be placed in their sockets and successively pushed in. CAUTION: make certain cards are centered in the sockets. Otherwise excessive force may be required to insert them.

POWER SUPPLY SERVICE All power supply components may be reached by removing the left side panel. This should be removed to replace the plug-in voltage regulator.

MEMORY BOARD SERVICE Remove top cover and rear panel. All components on the memory board may now be reached for probing. There is sufficient slack in the interconnect cables so that the three screws holding the memory board to the mother

board may be removed and the memory board be folded back so that the components are facing up.

MOTHER BOARD SERVICE

For access to the rear of the mother board, follow the memory board service procedure and, if necessary, the power supply service procedure. The mother board has few active components (other than the power supply) and should not be serviced unless all possibilities are exhausted. Note that this board is very thick for mechanical support, and components should be removed and replaced with caution to avoid damaging the plated through holes. This is especially true with regard to the module sockets.

BEZEL REMOVAL

The plexiglass bezel is permanently attached to the panel and should not be removed! If it becomes scratched or damaged and you wish to change it, call the factory for assistance. (Do not clean the bezel with strong solvents. Alcohol, Windex, Soap and Water, and Freon are OK. Do not use Ampex tape head cleaner!)

ADDING ADDITIONAL OUTPUTS

Additional output modules may be added in the field. When factory supplied, modules are in the following positions:

1 OUTPUT	POSITION 3
2 OUTPUT	POSITIONS 2, 4
3 OUTPUT	POSITIONS 1, 3, 5
4 OUTPUT	POSITIONS 1, 2, 4, 5
5 OUTPUT	ALL POSITIONS

For aesthetic and standardization considerations we recommend this scheme be followed.

Note that, to the right of all module sockets, near the bottom of the socket, is a 10K ¼watt resistor. This is installed for test purposes, as a partial bypass of the sequential timing circuit which is normally contained on each card. As factory supplied, sockets not containing cards have this resistor shorted. If cards are added or changed in position, this procedure must be followed:

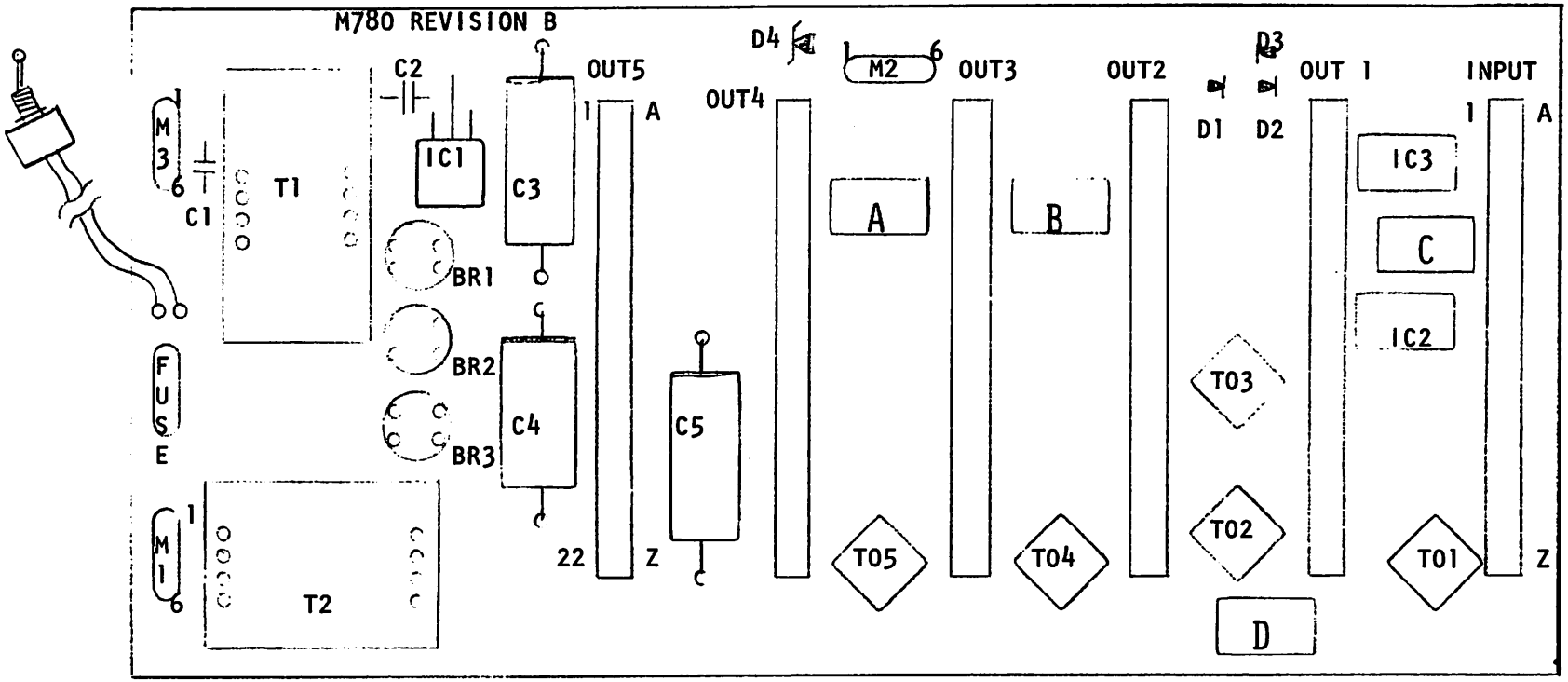
1: For output sockets 1 through 4, if a card is inserted in the socket, the resistor to its immediate right MUST NOT BE SHORTED.
2: For output sockets 1 through 4, if a card is NOT inserted in the socket, the resistor to its immediate right MUST BE SHORTED.
3: No resistor is required for socket 5.

To short the resistor, solder a short piece of wire across it on the front of the board.

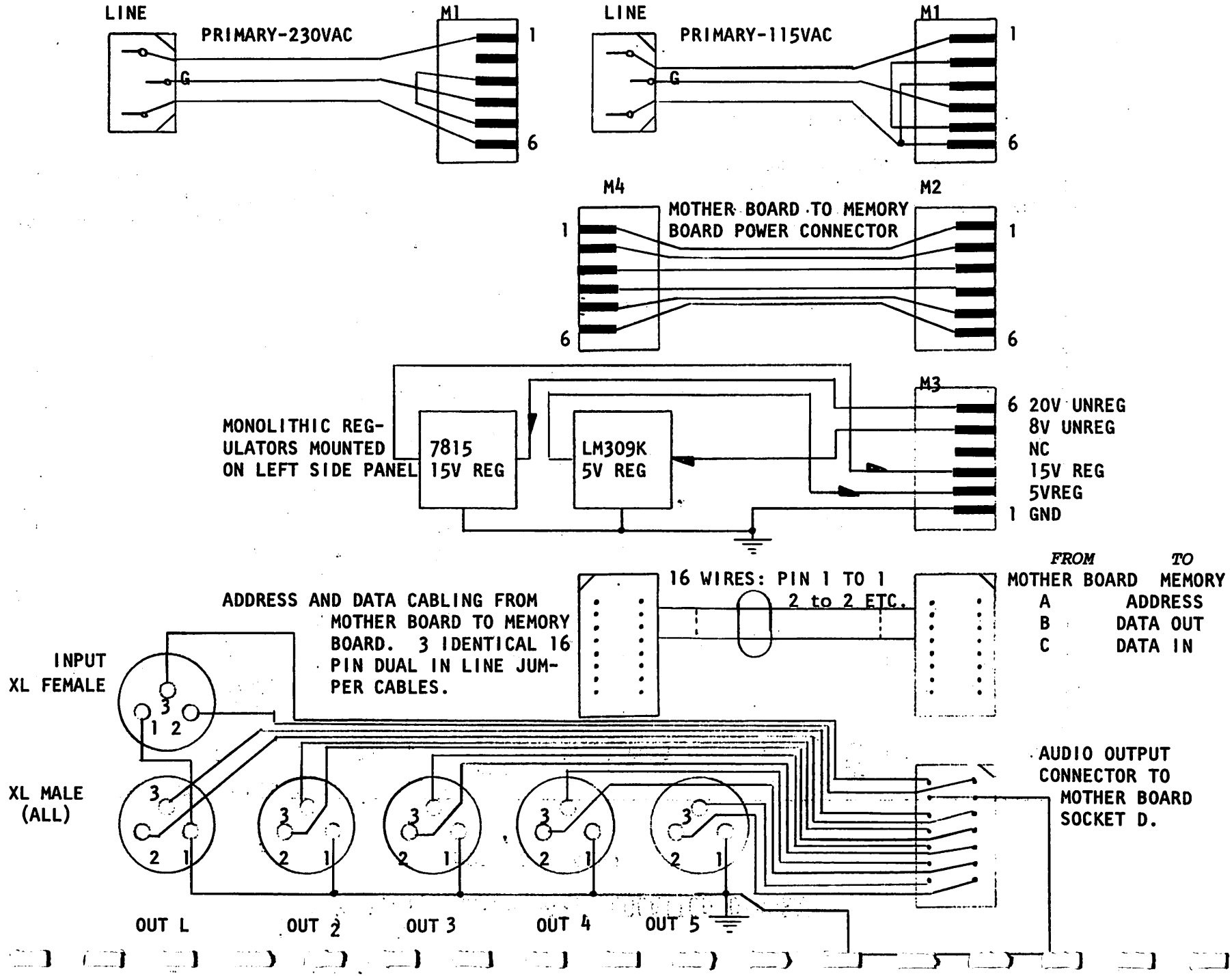
If output cards other than standard M694 assemblies are to be installed, be sure to refer to the instructions that are supplied either with the card, if purchased separately, or in the section of this manual devoted to that assembly.

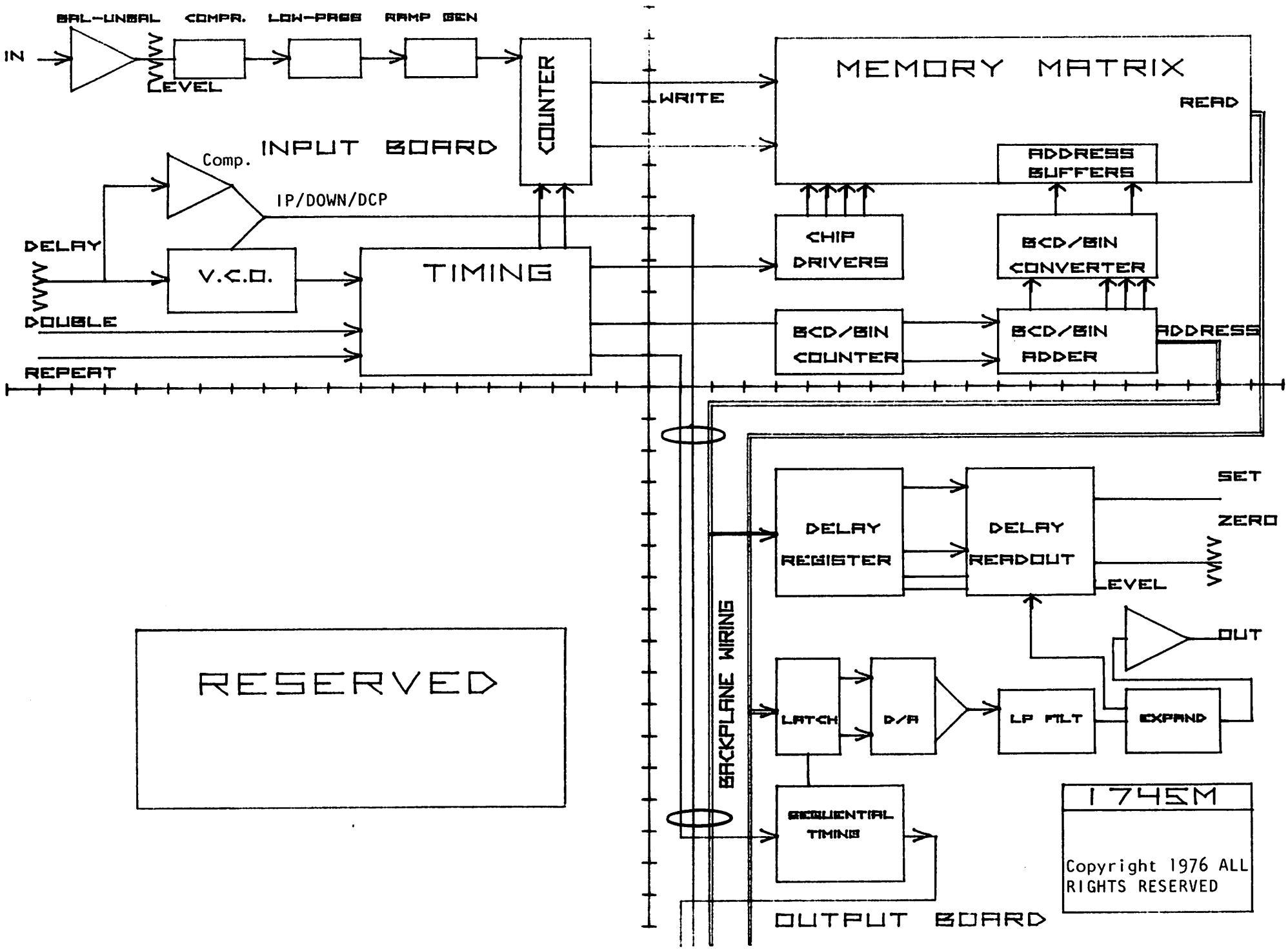
1745M MOTHER BOARD PARTS LOCATION DIAGRAM

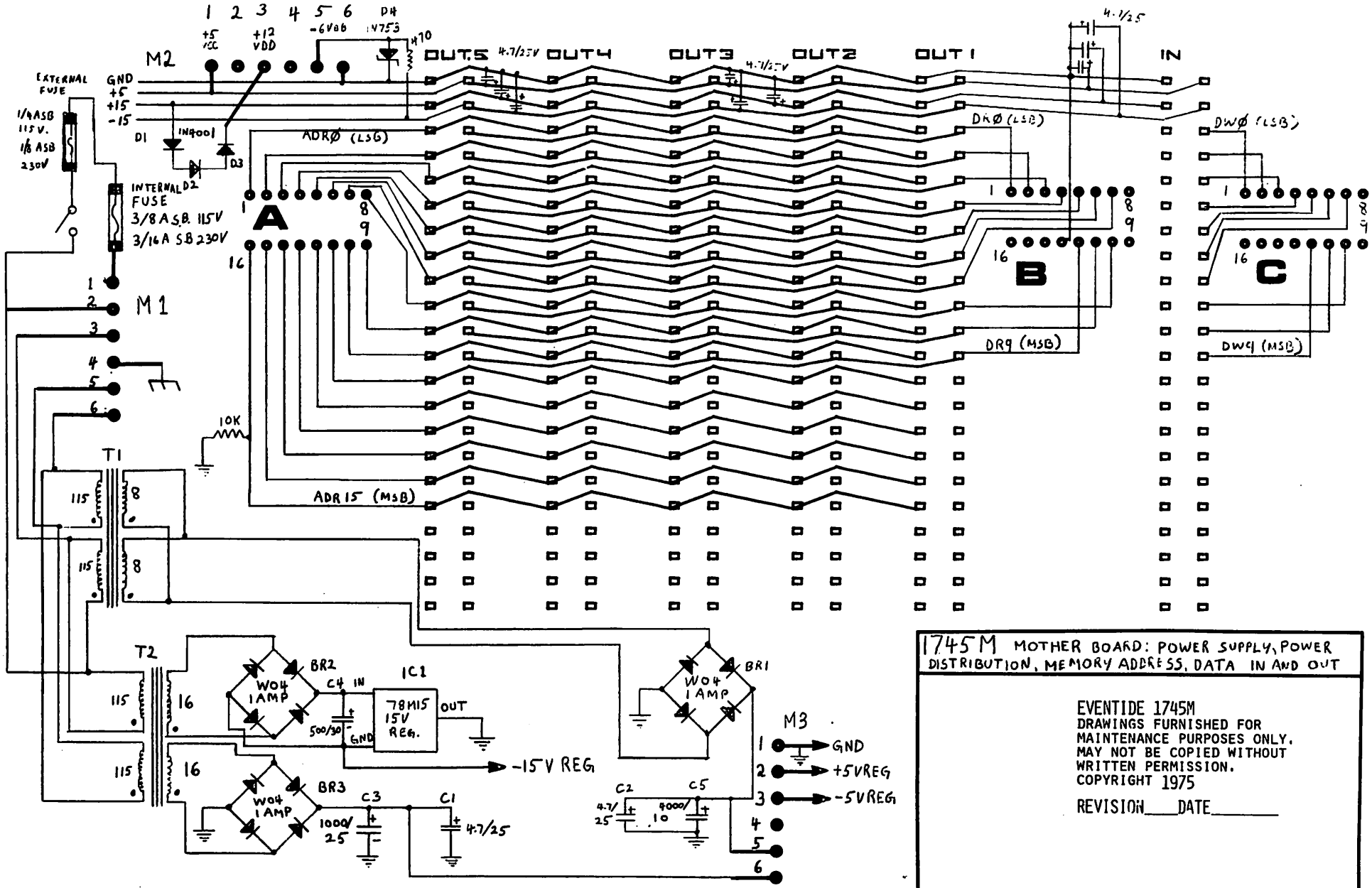
(NOT TO SCALE)



T01 through T05 are optional output transformers. Normally, jumpers are installed.

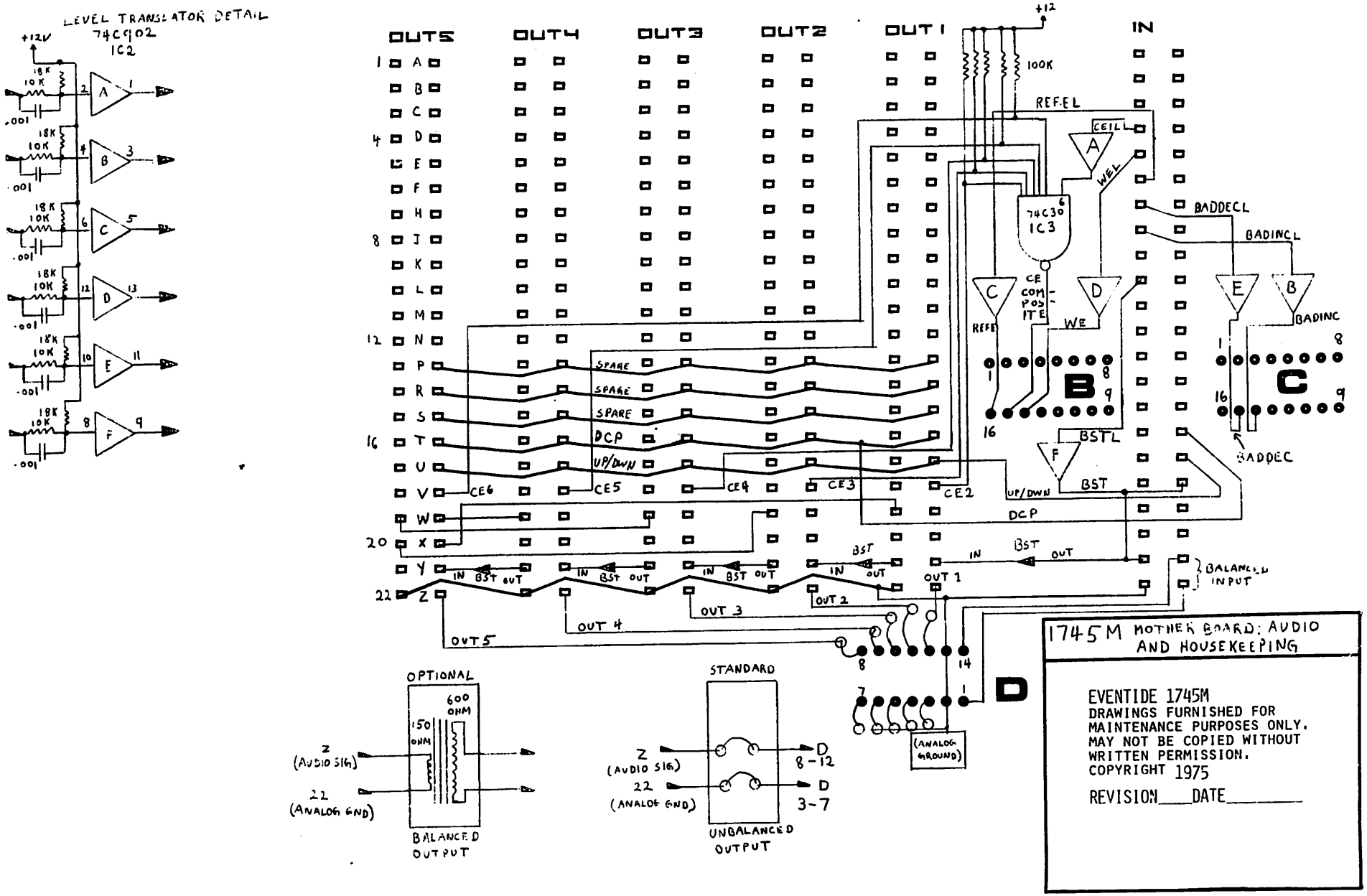

LINE
PRIMARY-230VAC
G
M1
1
6
LINE
PRIMARY-115VAC
G
M1
1
6
M4
1
6
MOTHER BOARD TO MEMORY BOARD POWER CONNECTOR
M2
1
6
MONOLITHIC REG-ULATORS MOUNTED ON LEFT SIDE PANEL
7815 15V REG
LM309K 5V REG
M3
6 20V UNREG
8V UNREG
NC
15V REG
5VREG
1 GND
ADDRESS AND DATA CABLING FROM MOTHER BOARD TO MEMORY BOARD. 3 IDENTICAL 16 PIN DUAL IN LINE JUM-PER CABLES.
16 WIRES: PIN 1 TO 1
2 to 2 ETC.
FROM TO
MOTHER BOARD MEMORY
A ADDRESS
B DATA OUT
C DATA IN
INPUT
XL FEMALE
3
1 2
XL MALE
(ALL)
3
2 1
AUDIO OUTPUT CONNECTOR TO MOTHER BOARD SOCKET D.
OUT L
OUT 2
OUT 3
OUT 4
OUT 5


BAL-UNBAL
COMPR.
LOW-PASS
RAMP GEN
IN
LEVEL
INPUT BOARD
COUNTER
WRITE
MEMORY MATRIX
READ
ADDRESS BUFFERS
Comp.
IP/DOWN/DCP
DELAY
V.C.O.
TIMING
CHIP DRIVERS
BCD/BIN CONVERTER
DOUBLE
REPEAT
BCD/BIN COUNTER
BCD/BIN ADDER
ADDRESS
RESERVED
DELAY REGISTER
DELAY READOUT
SET
ZERO
LEVEL
OUT
BACKPLANE WIRING
LATCH
D/A
LP FILT
EXPAND
SEQUENTIAL TIMING
OUTPUT BOARD
1745M
Copyright 1976 ALL RIGHTS RESERVED



1745M MOTHER BOARD: POWER SUPPLY, POWER DISTRIBUTION, MEMORY ADDRESS, DATA IN AND OUT

REVISION____DATE_____


LEVEL TRANSLATOR DETAIL
74C902
IC2
+12V
18K
10K
.001
OUT5
OUT4
OUT3
OUT2
OUT 1
IN
100K
REFEL
CEILL
WEL
74C30
IC3
BADDECL
BADINCL
CE COMPOSITE
REFE
WE
BSTL
BST
BADINC
BADDEC
SPARE
SPARE
SPARE
DCP
UP/DWN
CE6
CE5
CE4
CE3
CE2
IN BST OUT
OUT 1
OUT 2
OUT 3
OUT 4
OUT 5
BALANCED INPUT
OPTIONAL
600 OHM
150 OHM
Z (AUDIO SIG)
22 (ANALOG GND)
BALANCED OUTPUT
STANDARD
Z (AUDIO SIG)
22 (ANALOG GND)
D 8-12
D 3-7
UNBALANCED OUTPUT
(ANALOG GROUND)
1745M MOTHER BOARD: AUDIO AND HOUSEKEEPING
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MOTHER BOARD WIRING LIST M780 REVISION B

This sheet describes the interconnection between the various circuit assemblies which connect to the mother board. There are 6 dual 22pin edge connectors, one of which is designated as the INPUT socket, and the 5 remaining as OUTPUT sockets, 1 through 5. These 6 sockets receive individual input and output modules. There are 3 sockets which accept 16 pin jumper cables which interface with the MEMORY board. These sockets are labelled "A", "B", and "C", and have the following functions:

A: Convey the addresses generated by the various OUTPUT boards to the MEMORY board.
B: Receive the memory data output and distribute it to the OUTPUT boards which strobe it into their buffers.
C: Convey the data generated by the A-D converter, and certain control signals, to the MEMORY board.

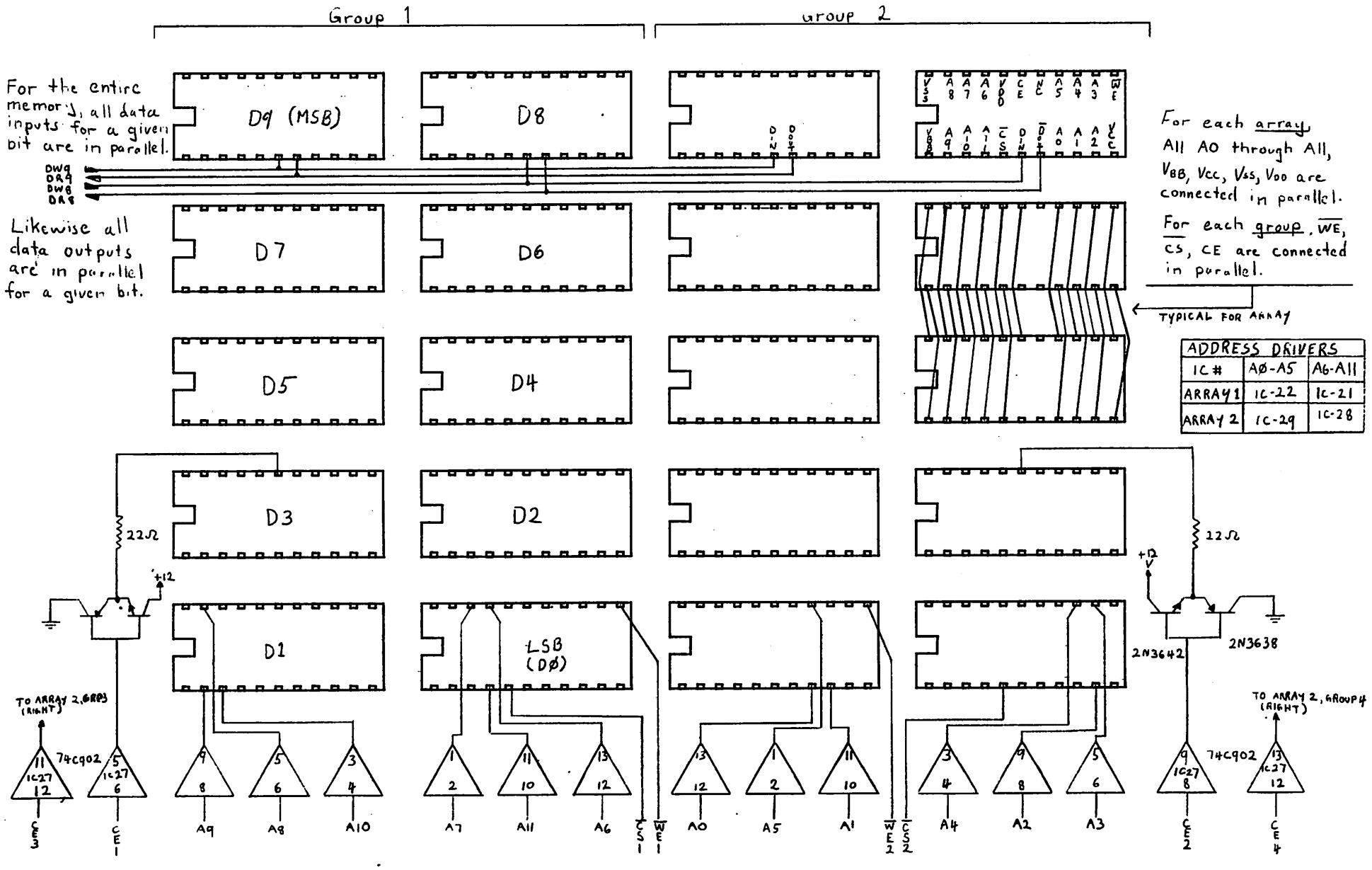
PIN	INPUT	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5
1	DIGITAL GROUND					
2	+15 VDC POWER DISTRIBUTION					
3	ADDRESS LSB			(ADR0)		
4	CEIL			(ADR1)		
5	WEL			(ADR2)		
6	REFEL			(ADR3)		
7	BADDECL			(ADR4)		
8	BADINCL			(ADR5)		
9	NC			(ADR6)		
10	BSTL			(ADR7)		
11	NC			(ADR8)		
12	NC			(ADR9)		
13	NC			(ADR10)		
14	NC			(ADR11)		
15	NC			(ADR12)		
16				(ADR13)		
17				(ADR14)		
18	ADDRESS MSB			(ADR15)		
19	NC	DELAY REMOTE CONTROL STROBE				DRCS3
20	NC	NC	NC	NC*	NC	DRCS2
21	BST OUT	BST OUT	BST OUT	BST OUT	BST OUT	NC
22	ANALOG GROUND					
A	+5VDC POWER DISTRIBUTION					
B	-15VDC POWER DISTRIBUTION					
C	DW0	DATA READ LSB		(DR0)		
D	DW1			(DR1)		
E	DW2			(DR2)		
F	DW3			(DR3)		
H	DW4			(DR4)		
J	DW5			(DR5)		
K	DW6			(DR6)		
L	DW7			(DR7)		
M	DW8			(DR8)		
N	DW9			(DR9)		
P	NC	SPARE				
R	NC	SPARE				
S	NC	SPARE				
T	DCP OUT			DCP IN		
U	UP/DWN OUT			UP/DWN IN		
V	BST OUT	CE2	CE3	CE4	CE5	CE6
W	NC	NC	NC	NC*	NC*	DRCS4
X	NC	NC	NC	NC*	NC	DRCS1
Y	ANALOG IN	BST IN	BST IN	BST IN	BST IN	BST IN
Z	ANALOG IN			ANALOG OUTPUT		

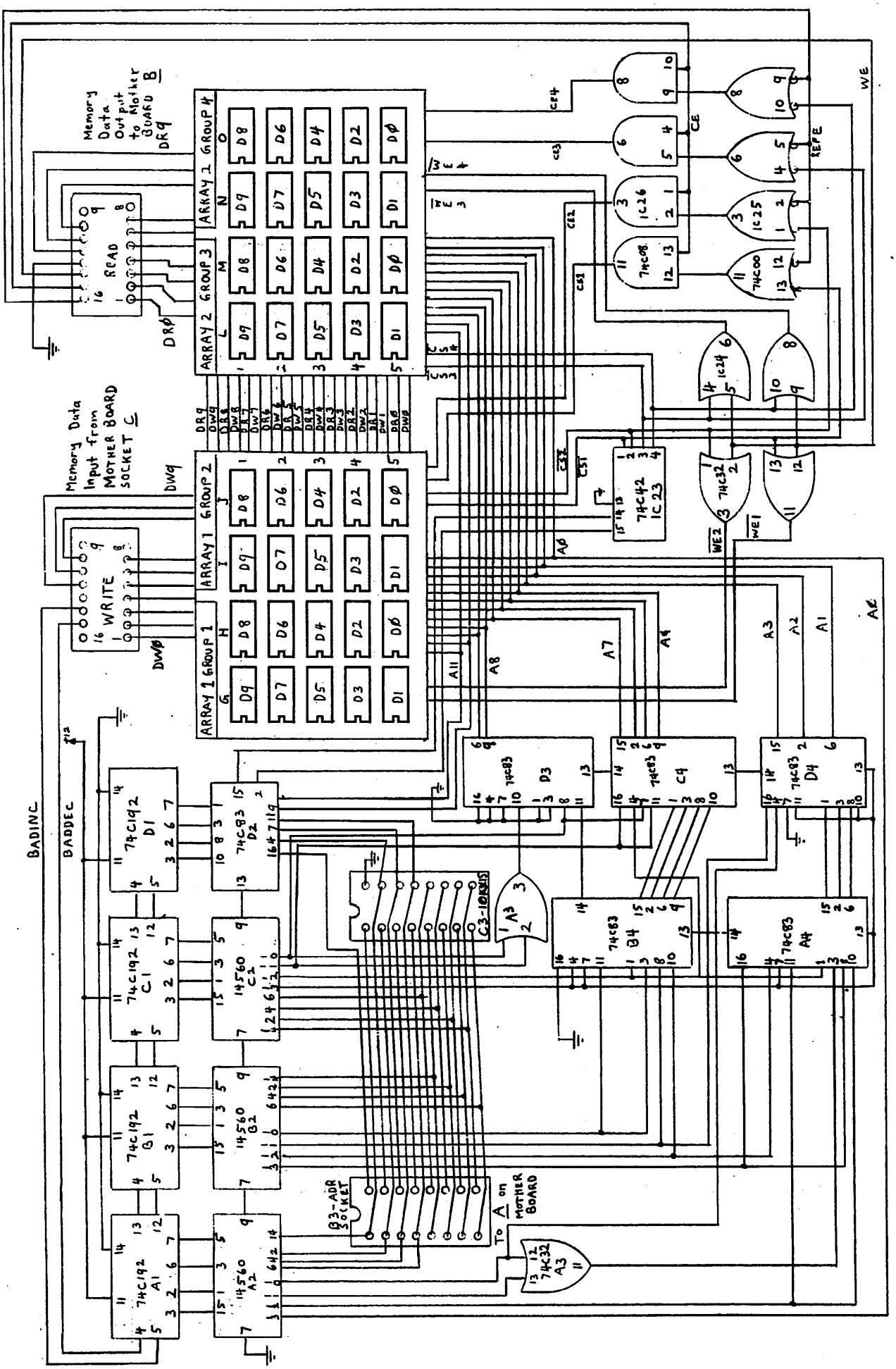
SOCKET B	A	C
DR0 (LSB)	ADR0	DW0
DR1	ADR1	DW1
DR2	ADR2	DW2
DR3	ADR3	DW3
DR4	ADR4	DW4
DR5	ADR5	DW5
DR6	ADR6	DW6
NC	ADR7	NC
NC	ADR8	NC
DR7	ADR9	DW7
DR8	ADR10	DW8
DR9 (MSB)	ADR11	DW9
DIG.GND.	ADR12	NC
WE	ADR13	BADINC
CE COMPOSITE	ADR14	BADDEC
REFE	ADR15	NC

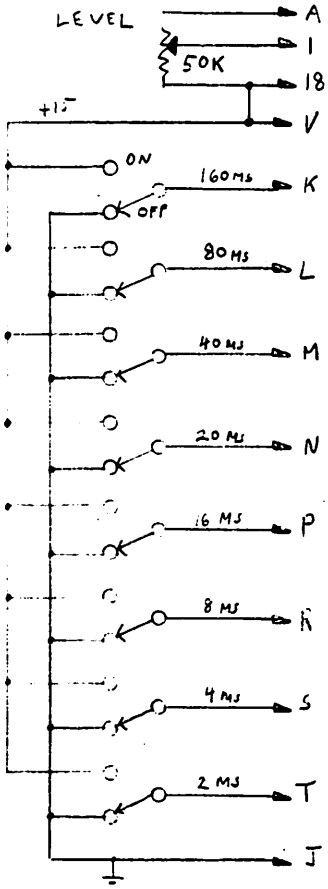
EVENTIDE 1745M

REVISION____DATE_____

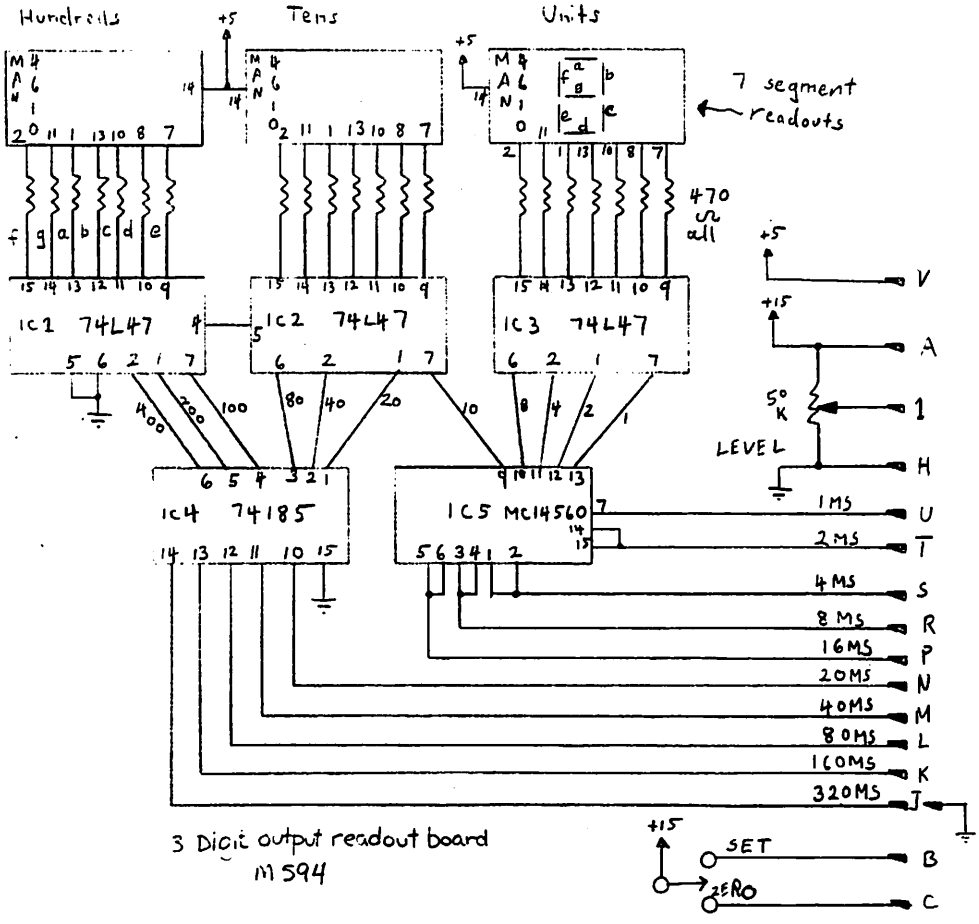
*USED AS TIE POINT


Group 1
Group 2
For the entire memory, all data inputs for a given bit are in parallel.
DWG
DRG
DWG
DRG
Likewise all data outputs are in parallel for a given bit.
D9 (MSB)
D8
D7
D6
D5
D4
D3
D2
D1
LSB (DØ)
DIN
DOUT
For each array, All AØ through A11, VBB, Vcc, Vss, Voo are connected in parallel.
For each group, WE, CS, CE are connected in parallel.
TYPICAL FOR ARRAY
ADDRESS DRIVERS
IC # | AØ-A5 | A6-A11
ARRAY 1 | IC-22 | IC-21
ARRAY 2 | IC-29 | IC-28
22Ω
+12
+Ω V
12Ω
2N3642
2N3638
TO ARRAY 2, GROUP 3 (RIGHT)
TO ARRAY 2, GROUP 4 (RIGHT)
74C902
IC27
A9
A8
A10
A7
A11
A6
A0
A5
A1
A4
A2
A3
CE3
CE1
CE2
CE4
CS1
WE1
WE2
CS2

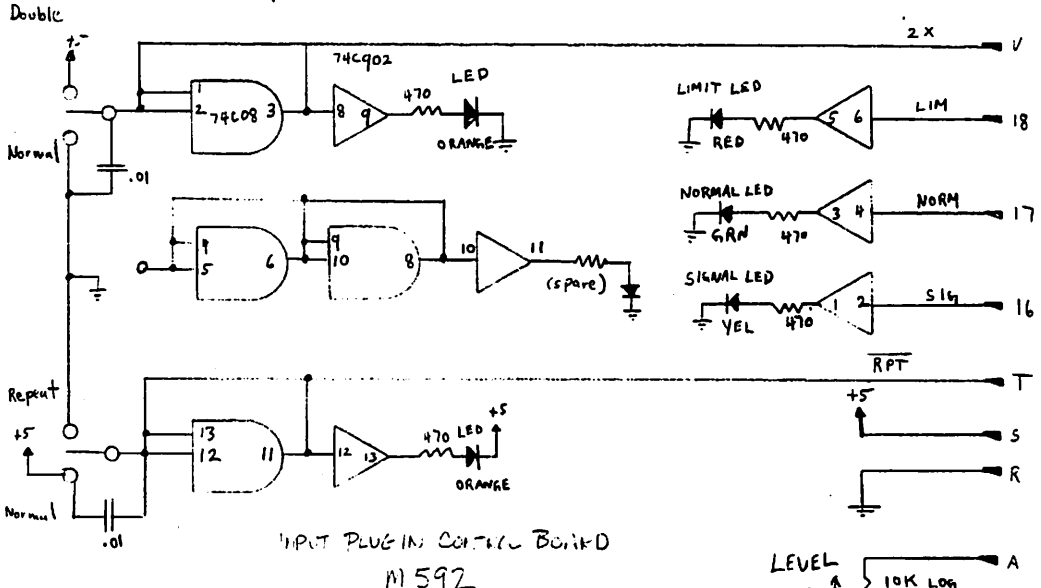

Memory Data Output to Mother Board B
16 READ 1
DRØ
DR9
ARRAY 2 GROUP 3
ARRAY 1 GROUP 2
ARRAY 1 GROUP 1
Memory Data Input from MOTHER BOARD SOCKET C
16 WRITE 1
DWØ
DW9
BADINC
BADDEC
74C192 D1
74C192 C1
74C192 B1
74C192 A1
14560 C2
14560 B2
14560 A2
74C83 D2
74C83 D3
74C83 C4
74C83 B4
74C83 A4
74C42 IC 23
74C32 A3
C3-ADR Socket
To A on MOTHER BOARD
WE
CE
REFE
WE2
WE1
CS4
CS3
CS2
CS1
A0
A1
A2
A3
A4
A7
A8
A9
A11
A12



SWITCH REGISTER BOARD
M591

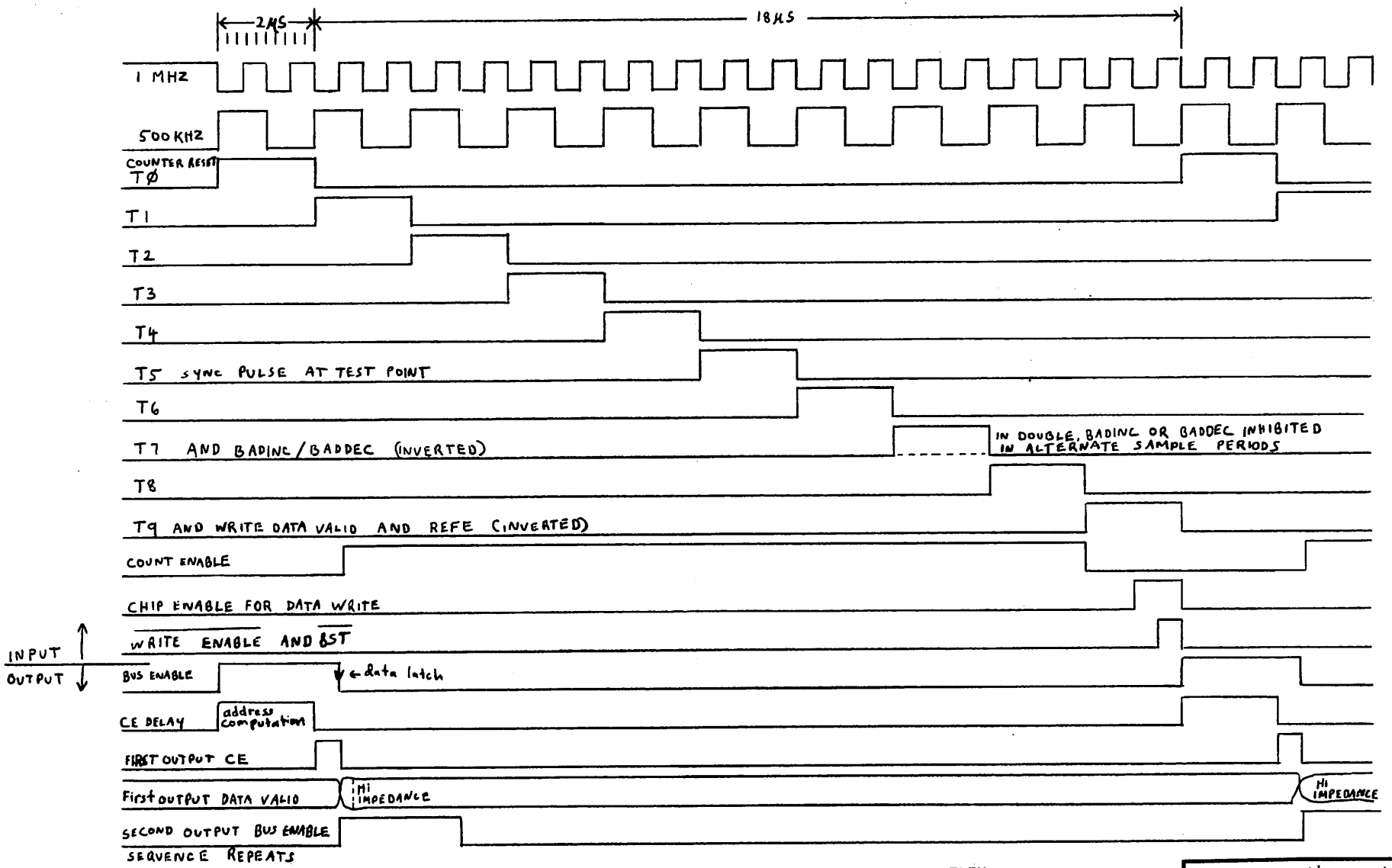


3 Digit output readout board
M594



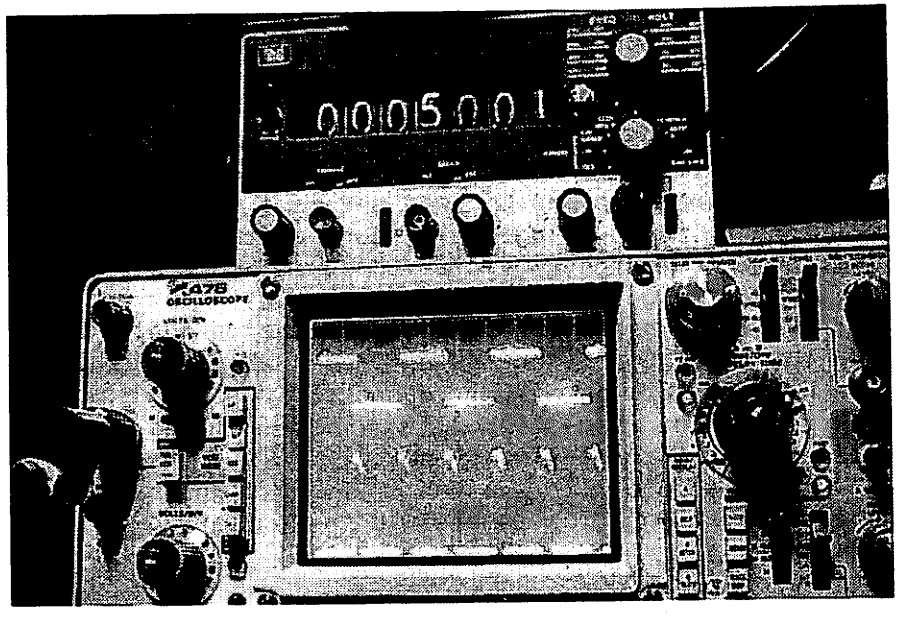
INPUT PLUG-IN CONTROL BOARD
M592

REVISION____DATE_____



1745M TIMING DIAGRAM

APPENDIX-----TROUBLESHOOTING TECHNIQUES



Observing high speed waveforms and making precise measurements requires special test equipment. The upper unit is a frequency counter capable of measuring a 50 MHz signal to an accuracy of 10Hz and a resolution of .1Hz. The oscilloscope has a bandwidth of 200MHz and can accurately reproduce pulses of only a few nanoseconds duration.

When probing closely packed IC packages, it is important to use low capacitance probes. Do not use the standard alligator clip on the end of a piece of coax! The CMOS circuits are especially sensitive to capacitive loading: they will slow down and critical timing will be disrupted. Invest in two good scope probes- they will pay for themselves in one troubleshooting session.

There are two types of digital circuits. There are "combinatorial" circuits, typified by the so-called "gate", whose output is directly dependent upon its inputs. And, there are "sequential" circuits, typified by the "flip-flop", which are dependent in part upon their inputs at the present time, and in part upon their inputs at some previous time.

Both of these circuits have a unifying characteristic—they are *fast*. While a single cycle of 1kHz tone meanders by, your common 20¢ gate can perform 20,000 logical operations. As long as it does these operations correctly, there is no problem. If it does 19,999 of these operations correctly and then makes a mistake, there most definitely is. Fortunately, you can sneak up and catch it making its mistake without specifically watching all 20,000 operations. In order to do this, a good oscilloscope is required.

The section detailing equipment required mentioned a wide bandwidth oscilloscope. In order to be able to see *everything* that goes on in the DDL, a 100MHz scope is necessary. Luckily, except for a few high frequency stages operating at 64MHz, most of the DDL runs at low megahertz and high kilohertz rates. Wide bandwidths are still necessary to view time relationships and let square waves look like square waves, but 10 to 20 MHz is adequate. If an audio bandwidth scope must be used, remember that square waves will be rounded, and the higher frequency timing signals will be severelyattenuated and, probably, hopelessly muddled. So it goes.

Scope synchronization is one of the most important aspects of troubleshooting. Digital waveforms are characterized by variable pulse widths, and signal lines which carry a few pulses and then remain dormant for a while. The scope should be triggered by the *least rapidly* occurring event in the system. For instance, the Chip Enable signal on the memory board is always present at a certain fixed time with respect to the sampling signal, and is present at other, variable times in between. If one tried to trigger the scope on the CE signal, triggering, and other waveforms being compared, would appear unstable. Some scopes, with variable trigger holdoff, can trigger on such waveforms, but a far better solution, is to use a stable trigger against which to compare other signals. Such a trigger may be obtained on the INPUT board, and a test point which goes true during T5 is made available near IC 16, and may be reached by removing the top cover of the DDL. A ground test point is also provided immediately adjacent to it, and should be used to prevent false triggering by noise. This signal occurs at a 50KHz rate and at a fixed relationship with the basic timing signals TØ through T9. If the scope has an external triggering input, use this, leaving both traces free for waveform observance.

The reason for the desirability of observing signals two at a time is inherent in the nature of the IC's being tested. The simplest IC, the "inverter", has an input that is the opposite level from the output. Look at the input on one scope channel and the output on another. The two should be inverted with respect to each other at all times. If they are not, it indicates either a defective inverter or a short-circuited output. Defective logic gates respond to the same treatment. In checking a 74C00, note that the output must be low if both inputs are high, and must be high if either or both inputs are low. Observe the output on one channel, and sequentially observe the inputs on the other, and make sure that this relationship obtains. Due to the persistence of the scope trace, one failure out of thouands is visible. The failed part of the trace will be dimmer than the good part, but will nonetheless be very obvious.

In logic circuit theory (and in this manual), the terms "1" and "TRUE" and "HIGH" are synonomous, as are "0", "FALSE", and "LOW". The 1 and 0 terminology is a harkening back to binary numbers and is generally used when discussing the outputs of counters and flip-flops. It is easier to say that the output state of a counter is 10010010 than "TRUEFALSEFALSETRUEFALSEFALSETRUEFALSE". The "TRUE" and "FALSE" terminology is sometimes more convenient when discussing gates or other devices which perform logical operations. For instance, in the NAND gate, the output is FALSE if the two inputs are TRUE. HIGH and LOW are referred to in measurement situations when one is observing a scope or a meter. A 1 or TRUE usually corresponds to a greater voltage level.

When designing digital systems, it is customary to give names to signals that must be continued from one portion of the circuit to another, or if they are particularly significant signals in the operation of the device. Typically, there are many more interconnections in a digital system than in an analog one, and individual circuit blocks may transmit parallel digital signals to succeeding ones, as opposed to single signals in audio systems. These signal names are known as "Mnemonics", after Mnemosyne, the Greek goddess of spaghetti. Legend has it that when the first computer was built, the circuit diagrams looked so much like spaghetti that some way had to be found to simplify them, and the naming of the signals was the result. Idealy, the names assist in interpreting and remembering the function of the signal. The signal "ADRØ", reasonably enough, refers to the address bus line carrying the least significant bit of address data. In large, multiboard systems, these mnemonics tend to proliferate and grow prefixes and suffixes like a German lexicologist with echolalia.

The 1745M requires very few mnemonics. As it is a bus oriented system, the three main signals are in groups. They are:

ADRØ through ADR15. These are the various address lines that select the delay, and are generated by each of the output boards in turn, and received by the memory board.

DWØ through DW9. These are the Data Write signals generated in the input board, and are written in the memory.

DRØ through DR9. These are the Data Read signals generated by the RAM's, and are received by the output boards in turn.

In each case, the lower numbers represent the least significant bits. These three groups of mnemonics account for 36 separate signal lines, and may be considered the data flow through the DDL.

There are a few more, mostly concerned with driving the memory, and they are described in the circuit descriptions.

Digital IC's come in "families". Each family has its advantages and disadvantages. The major families used in the Eventide 1745M are known as MOS (Metal Oxide Semiconductor), and CMOS (ComplementaryMOS). There are also a scattering of Schottky TTL (Transistor-Transistor Logic) and even one lonely TTL. This is a distinct departure from past designs which in recent years were almost exclusively TTL. The reason is that the price of CMOS logic, which was just introduced in the early 1970's, became reasonable enough to allow it to be used in non-military designs. CMOS is a form of logic that uses complementary field effect transistors for switching. It has extremely high input impedance, with the result that, its power consumption which it is not actually switching, is equal to the leakage currents associated with the FET's. For this reason, low speed circuits, such as the delay registers on the output boards have current drains measured in microamps. And CMOS is also used to perform arithmetic operations on the RAM board, where it moves along fairly fast, and still requires an order of magnitude lower power than TTL. The almost exclusive use of this logic family allowed us to reduce total power requirements by over 75%, and eliminate the necessity for a heat sink and special precautions for ventilation, The other major family used, MOS, is employed in the random access memory chips. This technology is similar to that used in shift registers, but some power saving is obtained because they are operated in parallel, and so clocking speed is reduced substantially.

Troubleshooting the CMOS circuits is a bit involved because there are many different types. The first step is to understand what the particular chip does in the system. In the case of gates, an understanding of the truth table is imperative. In the case of counters and flip-flips, check to see if the proper output changes follow clock and reset pulses. The most difficult parts to check are the adders on the RAM board. Although these chips are just large assortments of gates, their internal connections are not available for probing, and their truth tables are quite complicated. Most failures will involve external nodes, and the first thing to check is that all inputs and outputs do have clearly defined logic level signals. CMOS swings directly between the positive and negative power supply rails, and if any signal appears too low, it is an immediate cause for suspicion. The best tool for checking the RAM addressing section is a logic analyzer, and if you have one, you're certainly not reading this section!

Troubleshooting the RAM's is a lot easier than it would seem at first glance. Even though the inputs, outputs, and addresses are in parallel, it is frequently possible to find a defective chip in a minute or less. A convenient procedure is detailed below:

STEP:	ACTION
1:	Set all delays at zero and listen to output with signal applied. (Low level 1kHz sine wave ideal, unless problem only appears at high level.)
2:	Does the signal get noisy and then clear up about three times a second? (Noise level may be very high or almost inaudible, depending upon which bit is affected.)
3:	If noise is continuous, it is probably NOT a defective RAM. If problem is as step 2 suggests, increase the delay. If there is a change in the noise, the problem may be in the addressing circuitry. If no change, proceed to step 4.
4:	Observe signal at output D/A converter test point, and adjust sine wave level until noise is about 1/4 as large as peak to peak signal. It should now be possible to see it coming and going. Determine by the relative signal level approximately which bit is involved.
5:	Look at the input signal to that bit on any of the memories, and after you know the pattern, look at the output signal on the same chip. For this test, the scope should be synchronized to the audio input, and the delays set at zero, so a stationary pattern is obtained.
6:	Check bits higher and lower than your guess until you see a memory output whose pattern changes when the noise appears. This narrows the problem down to the four chips with the same bit number as shown on the memory schematic.
7:	Finally, while listening to or watching the output, look at the chip select signal in each of the four memory groups. These signals have a duty cycle 3/4 high, 1/4 low. Look for the one that is low when the noise is present. (This may be easier to see in the DOUBLE mode).
8:	The RAM in the group as just determined with the bit number as determined in step 6 is the evildoer.

Note that massive failures in the memory are extremely unlikely to be the fault of a signle RAM. If several bits appear to be defective by the above criteria, look for improper chip enable, chip select, and address levels.

The above hints should be helpful to the analog person in the DDL's digital world. If you have any questions pertaining to fixing the DDL that aren't covered by this manual or the appendix, feel free to call the factory. (See *What to do if All Else Fails).*

WHAT TO DO IF ALL ELSE FAILS

Although the data in the Technical Information section is sufficient to enable a competent technician to maintain and repair the Delay Line, we recognize that not all problems can be solved immediately in "the field". For instance, certain components may be difficult or impossible to obtain through normal distributor channels. If a component should fail, first try to obtain it locally. This pertains especially to standard devices such as resistors, capacitors, transistors, and operational amplifier IC's. To facilitate this, the schematics have been deliberately marked with generic types rather than manufacturer's part numbers. Thus, a Motorola type MLM301AP1 becomes a "301", replaceable with a similar part by Fairchild, National, or any other alternate source.

Two components used in substantial volume are the 22 pin RAM's and 1.5µf dipped tantalum bypass capacitors. If a RAM should fail, an extensive table of replacements may be found in the circuit description section. If a tantalum bypass should fail, it may be replaced by one of similar voltage rating but almost any capacitance value. The only critical analog components are in the filter circuitry, and they are unlikely to fail.

If a capacitor or rectifier in the power supply fails, it may be replaced with a similar unit. In an emergency, the bridge rectifiers may be replaced by four rectifier diodes properly connected.

As the DDL is of largely modular construction, it is possible to replace a complete module instead of attempting to repair it. We recommend this in the case of the compressor/expander module. In most cases, the factory can supply a replacement module within a few hours plus shipping time. In an emergency, call the factory as described below, and we will do our best to help. *IMPORTANT:* If you want us to replace a module immediately, at no charge, you must have <u>previously</u> filled out the warranty sheet, so that we can confirm that you are entitled to the module. Otherwise, we will send the module COD and issue an appropriate refund when the defective is returned.

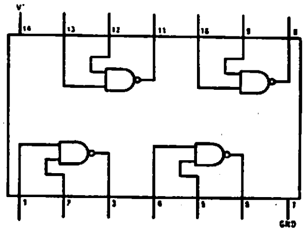
We can also supply some of the more difficult to find parts on a moment's notice, and will be pleased to do so upon request.

If you find it necessary to return equipment to the factory for repair, be sure to include complete shipping instructions and a description of any faults observed. If the defect is intermittent, clearly indicate under what circumstances and how frequently it appears. (We have an unusual habit of returning equipment the same day it comes in. We know you want it back, and we like to get it out quickly. Under such circumstances, an intermittent that you don't tell us about can get missed.)

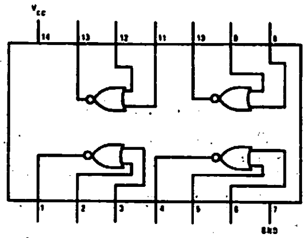
IN CASE OF EMERGENCY: We realize that our equipment is used in recording studios and at live concerts, and such enterprises are not time conscious in the normal "business hours" sense. If your equipment has problems which must be solved immediately, call our technical service number 212 581-9138 *any hour of the day or night.* (If it is an hour of the night, talk long enough to make sure the answerer is rational before asking questions.) To save time, it would be a good idea to have the equipment and test equipment set up near the phone before calling.

IN CASE OF NOT EMERGENCY: We will still be happy to talk to you. Please call 212 581-9290 during working hours, typically 9AM to 9PM, New York time.

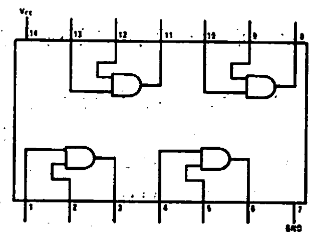
74C--- CIRCUITS USED IN 1745M



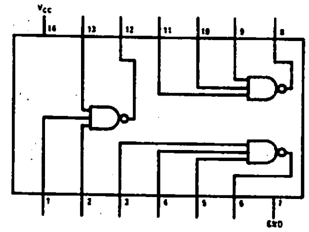
MM54C00/MM74C00
Quad 2-Input NAND Gate



MM54C02/MM74C02
Quad 2-Input NOR Gate

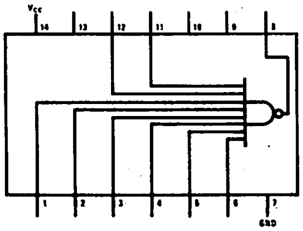


MM54C08/MM74C08
Quad 2-Input AND Gate

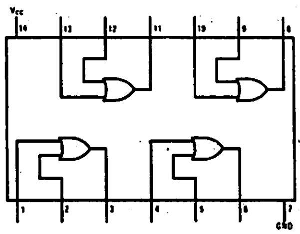


MM54C10/MM74C10
Triple 3-Input NAND Gate

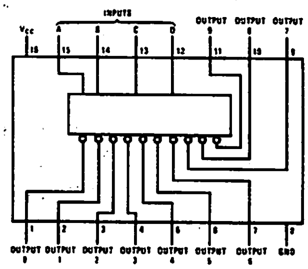
INPUTS D C B A	OUTPUTS 0 1 2 3 4 5 6 7 8 9
0 0 0 0	0 1 1 1 1 1 1 1 1 1
0 0 0 1	1 0 1 1 1 1 1 1 1 1
0 0 1 0	1 1 0 1 1 1 1 1 1 1
0 0 1 1	1 1 1 0 1 1 1 1 1 1
0 1 0 0	1 1 1 1 0 1 1 1 1 1
0 1 0 1	1 1 1 1 1 0 1 1 1 1
0 1 1 0	1 1 1 1 1 1 0 1 1 1
0 1 1 1	1 1 1 1 1 1 1 0 1 1
1 0 0 0	1 1 1 1 1 1 1 1 0 1
1 0 0 1	1 1 1 1 1 1 1 1 1 0
1 0 1 0	1 1 1 1 1 1 1 1 1 1
1 0 1 1	1 1 1 1 1 1 1 1 1 1
1 1 0 0	1 1 1 1 1 1 1 1 1 1
1 1 0 1	1 1 1 1 1 1 1 1 1 1
1 1 1 0	1 1 1 1 1 1 1 1 1 1
1 1 1 1	1 1 1 1 1 1 1 1 1 1



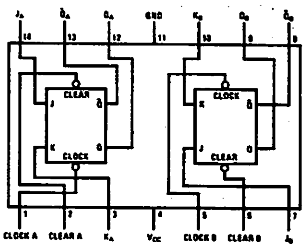
MM54C30/MM74C30†
8-Input NAND Gate



MM54C32/MM74C32†
Quad 2-Input OR Gate



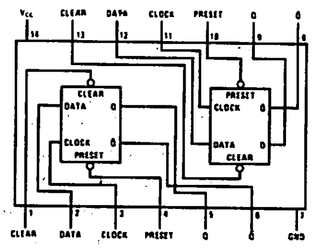
MM54C42/MM74C42
BCD to Decimal Decoder



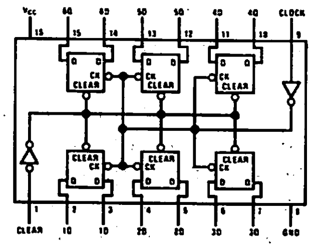
MM54C73/MM74C73
Dual J-K M/S Flip Flop

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

t_n = bit time before clock pulse.
t_{n+1} = bit time after clock pulse.



MM54C74/MM74C74
Dual D Flip-Flop

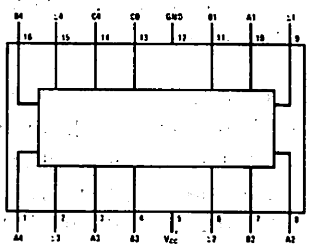


MM54C174/MM74C174†
Hex D Flip-Flop

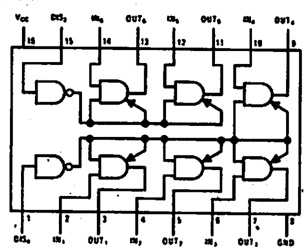
FUNCTION TABLE

INPUT				OUTPUT: WHEN C0 = L / WHEN C2 = L			OUTPUT: WHEN C0 = H / WHEN C2 = H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

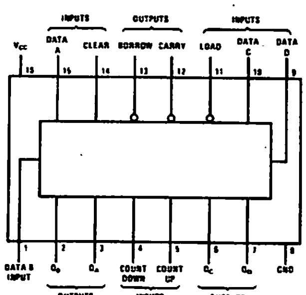
MM54C83/MM74C83
4-bit Binary Full Adder



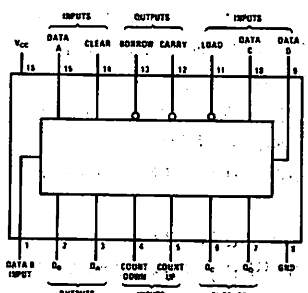
NOTE:
Input conditions at A3, A2, B2 and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.



MM70C97/MM80C97
TRI-STATE Hex Buffer

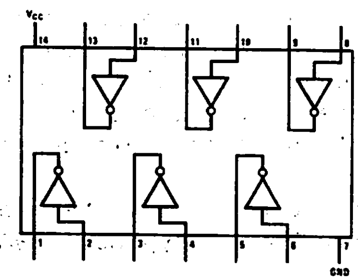


MM54C192/MM74C192
Synchronous Up/Down Decade Counter

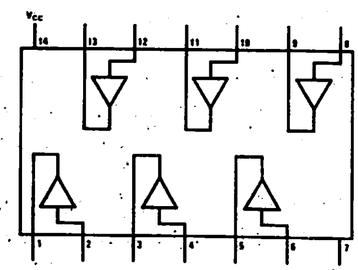


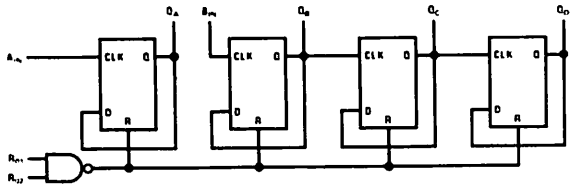
MM54C193/MM74C193
Synchronous Up/Down Binary Counter

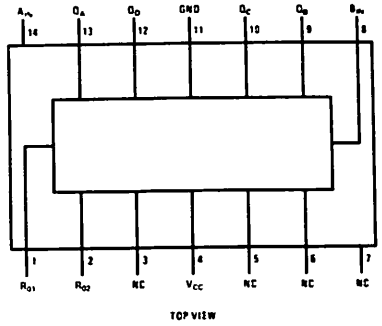
MM54C901/MM74C901
MM54C903/MM74C903

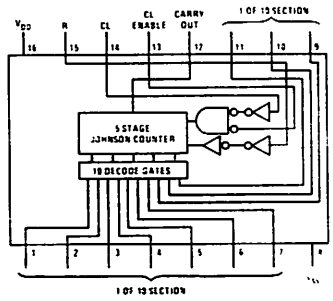


MM54C902/MM74C902
MM54C904/MM74C904





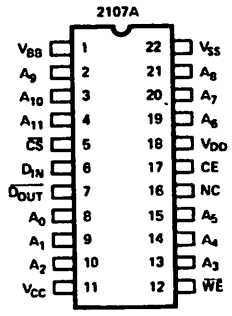




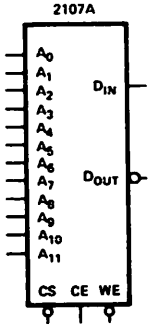
MM4617A/CD4017A
Decade Counter/Divider
Plus 10 Decoded Decimal Outputs

22PIN RANDOM ACCESS MEMORY

PIN CONFIGURATION



LOGIC SYMBOL

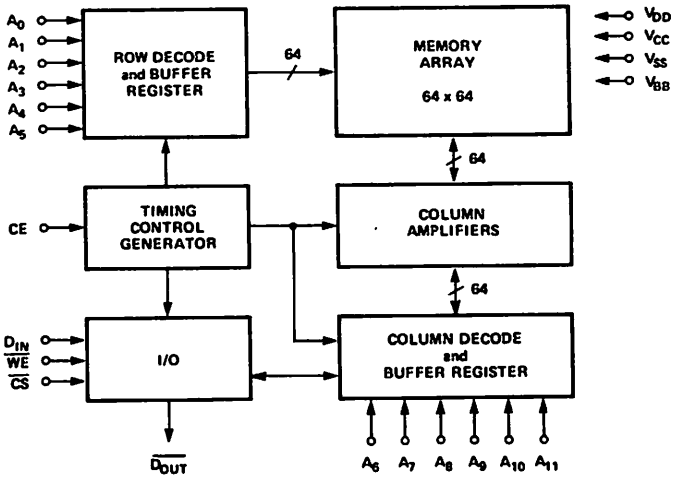


PIN NAMES

D_{IN}	DATA INPUT	CE	CHIP ENABLE
A_0-A_{11}	ADDRESS INPUTS*	$\overline{D_{OUT}}$	DATA OUTPUT
$\overline{WE}$	WRITE ENABLE	V_{CC}	POWER (+5V)
$\overline{CS}$	CHIP SELECT	NC	NOT CONNECTED

*Refresh Addresses A_0-A_5.

TYPICAL OF MANY MANUFACTURERS BLOCK DIAGRAM



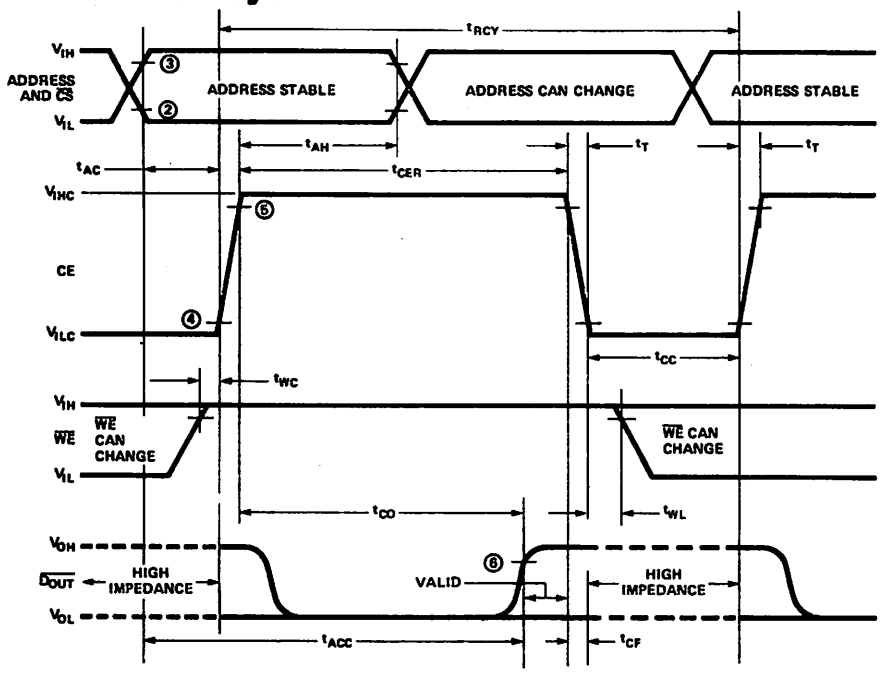
READ CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RCY}	Read Cycle Time	690		ns	t_T = 20ns
t_{CER}	CE On Time During Read	400	3000	ns	
t_{CO}	CE Output Delay		400	ns	C_{load} = 50pF, Load = One TTL Gate,
t_{ACC}	Address to Output Access		420	ns	Ref = 2.0V for High, 0.8V for Low.
t_{WL}	CE to $\overline{WE}$	0		ns	$t_{ACC} = t_{AC} + t_{CO} + 1t_T$
t_{WC}	$\overline{WE}$ to CE on	0		ns	

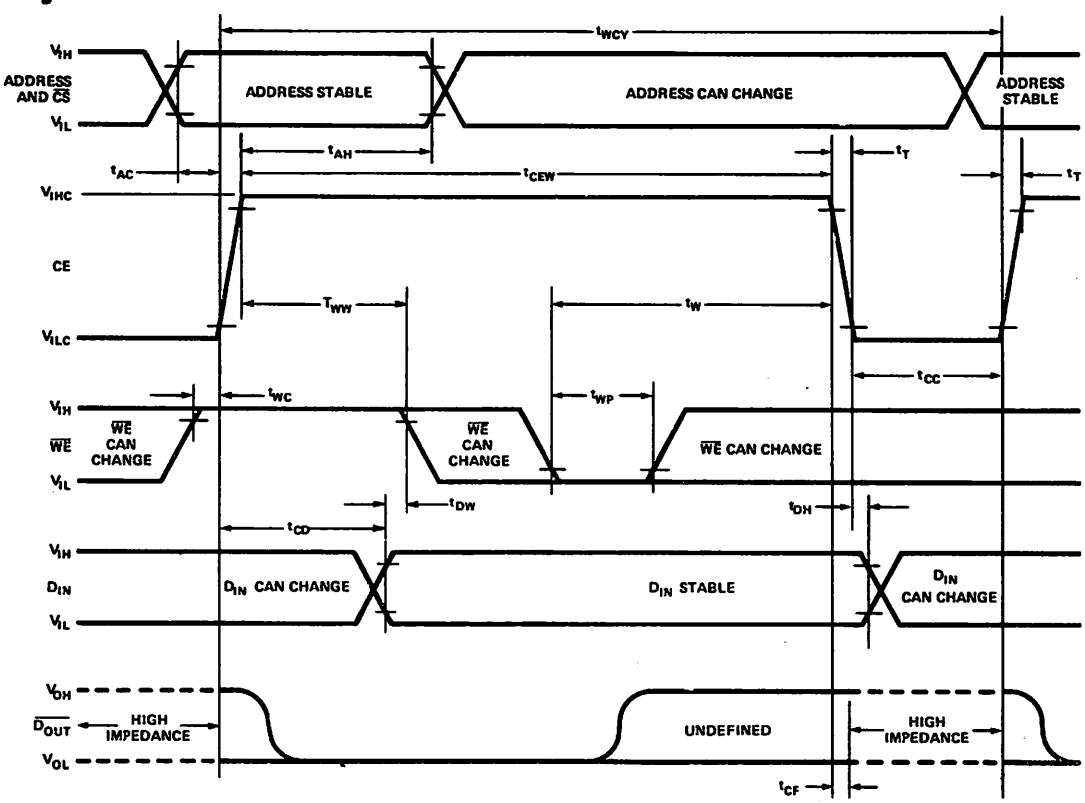
WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{WCY}	Write Cycle Time	970		ns	t_T = 20ns
t_{CEW}	CE Width During Write	680	3000	ns	
t_W	$\overline{WE}$ to CE Off	450		ns	
t_{WP}	$\overline{WE}$ Pulse Width	200		ns	
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		ns	
t_{CD} [1]	CE to D_{IN} Set Up		50	ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{WW}	$\overline{WE}$ Wait	200		ns	
t_{WC}	$\overline{WE}$ to CE On	0		ns	

Read and Refresh Cycle [1]



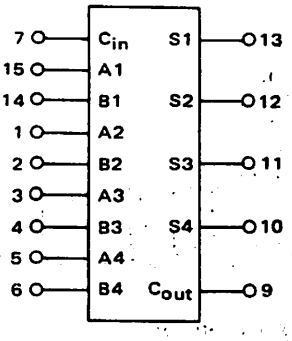
Write Cycle



NOTES:
1. For Refresh cycle row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
2. V_{SS} + 1.5V is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{SS} + 3.0V is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} + 2.0V is the reference level for measuring timing of CE.
5. V_{DD} -2V is the reference level for measuring timing of CE.
6. V_{SS} + 2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$.

BLOCK DIAGRAM

(LOW-POWER COMPLEMENTARY MOS)



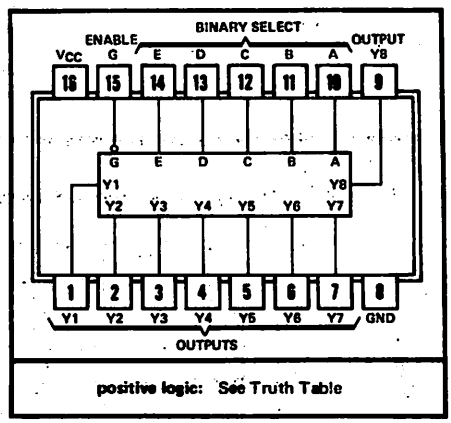
V_{DD} = Pin 16
V_{SS} = Pin 8

NBCD ADDER

MC14560CP

INPUT									OUTPUT				
A4	A3	A2	A1	B4	B3	B2	B1	C_{in}	C_{out}	S4	S3	S2	S1
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	1	0	0	0	0	1	1	0	0	0	1	1	1
0	1	0	0	0	0	1	1	1	0	1	0	0	0
0	1	1	1	0	1	0	0	0	1	0	0	0	1
0	1	1	1	0	1	0	0	1	1	0	0	1	0
1	0	0	0	0	1	0	1	0	1	0	0	1	1
0	1	1	0	1	0	0	0	0	1	0	1	0	0
1	0	0	1	1	0	0	1	1	1	1	0	0	1

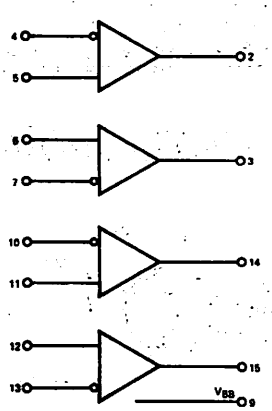
BINARY WORDS	INPUTS						OUTPUTS							
	BINARY SELECT					ENABLE								
	E	D	C	B	A	G	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0-1	L	L	L	L	L	L	H	H	L	L	L	L	L	L
2-3	L	L	L	L	H	L	H	H	L	L	L	L	L	H
4-5	L	L	L	H	L	L	H	H	L	L	L	L	H	L
6-7	L	L	L	H	H	L	H	H	L	L	L	L	H	H
8-9	L	L	H	L	L	L	H	H	L	L	L	H	L	L
10-11	L	L	H	L	H	L	H	H	L	L	H	L	L	L
12-13	L	L	H	H	L	L	H	H	L	L	H	L	L	H
14-15	L	L	H	H	H	L	H	H	L	L	H	L	H	L
16-17	L	H	L	L	L	L	H	H	L	L	H	L	H	H
18-19	L	H	L	L	H	L	H	H	L	L	H	H	L	L
20-21	L	H	L	H	L	L	H	H	L	H	L	L	L	L
22-23	L	H	L	H	H	L	H	H	L	H	L	L	L	H
24-25	L	H	H	L	L	L	H	H	L	H	L	L	H	L
26-27	L	H	H	L	H	L	H	H	L	H	L	L	H	H
28-29	L	H	H	H	L	L	H	H	L	H	L	H	L	L
30-31	L	H	H	H	H	L	H	H	L	H	H	L	L	L
32-33	H	L	L	L	L	L	H	H	L	H	H	L	L	H
34-35	H	L	L	L	H	L	H	H	L	H	H	L	H	L
36-37	H	L	L	H	L	L	H	H	L	H	H	L	H	H
38-39	H	L	L	H	H	L	H	H	L	H	H	H	L	L
40-41	H	L	H	L	L	L	H	H	H	L	L	L	L	L
42-43	H	L	H	L	H	L	H	H	H	L	L	L	L	H
44-45	H	L	H	H	L	L	H	H	H	L	L	L	H	L
46-47	H	L	H	H	H	L	H	H	H	L	L	L	H	H
48-49	H	H	L	L	L	L	H	H	H	L	L	H	L	L
50-51	H	H	L	L	H	L	H	H	H	L	H	L	L	L
52-53	H	H	L	H	L	L	H	H	H	L	H	L	L	H
54-55	H	H	L	H	H	L	H	H	H	L	H	L	H	L
56-57	H	H	H	L	L	L	H	H	H	L	H	L	H	H
58-59	H	H	H	L	H	L	H	H	H	L	H	H	L	L
60-61	H	H	H	H	L	L	H	H	H	H	L	L	L	L
62-63	H	H	H	H	H	L	H	H	H	H	L	L	L	H
ALL	X	X	X	X	X	H	H	H	H	H	H	H	H	H



74185

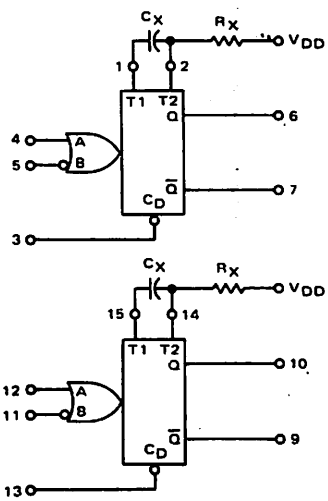
QUAD DIFFERENTIAL LINE RECEIVER

10115



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = "1"

MC14528
Dual Retriggerable/Resettable Monostable Multivibrator

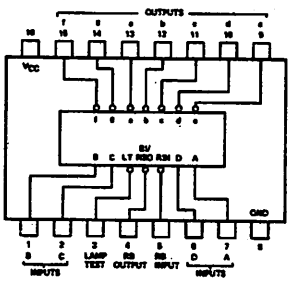


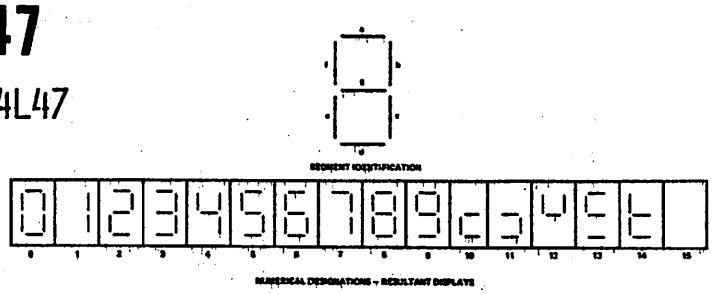
R_X and C_X are external components.

V_{DD} = Pin 16
V_{SS} = Pin 8

7447

AND 74L47





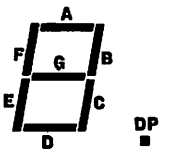
DESCRIPTION

The 7446 and 7447 BCD-to-Seven Segment Decoder/Driver are TTL monolithic devices consisting of the necessary logic to decode a BCD code to seven segment readout plus selected signs.

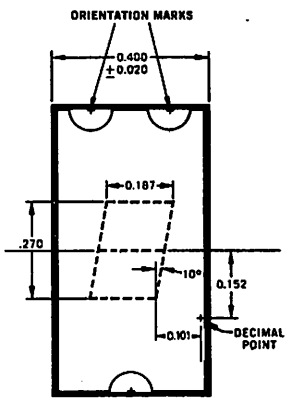
Incorporated in this device is a blanking circuit allowing leading and trailing zero suppression. Also included is a lamp test control to turn on all segments.

The 7446 and 7447 provide bare collector output transistors for directly driving lamps. The output transistor breakdown of the 7446 is 30 volts and the 7447 is 15 volts.

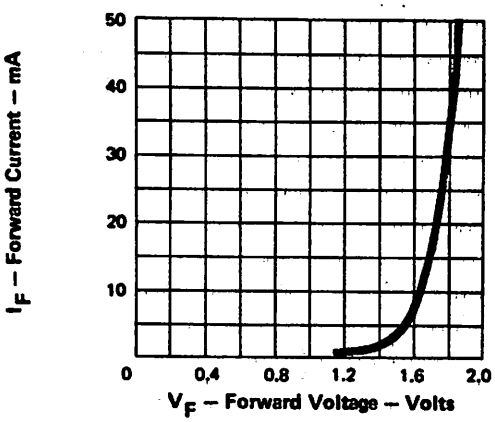
1. BI/BRO is wire-OR logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input must be open or held at a logical 1 when output functions 0 through 15 are desired and ripple-blanking input (RBI) must be open or at a logical 1 during the decimal 0 input. X = input may be high or low.
2. When a logical 0 is applied to the blanking input (forced condition) all segment outputs go to a logical 1 regardless of the state of any other input condition.
3. When ripple-blanking input (RBI) is at a logical 0 and A = B = C = D = logical 0, all segment outputs go to a logical 1 and the ripple-blanking output goes to a logical 0 (response condition).
4. When blanking input/ripple-blanking output is open or held at a logical 1, and a logical 0 is applied to lamp-test input, all segment outputs go to a logical 0.



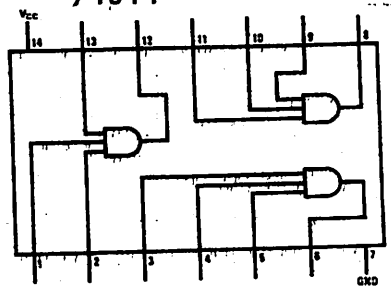
PIN 1 — CATHODE A
PIN 2 — ANODE A,F
PIN 3 — CATHODE F
PIN 4 — CATHODE G
PIN 5 — OMITTED
PIN 6 — CATHODE E
PIN 7 — ANODE D,E, DECIMAL
PIN 8 — CATHODE D
PIN 9 — CATHODE C
PIN 10 — CATHODE DECIMAL
PIN 11 — OMITTED
PIN 12 — OMITTED
PIN 13 — ANODE B,C,G
PIN 14 — CATHODE B



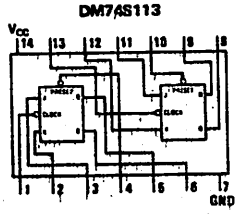
Forward Current (I_F) Versus Forward Voltage (V_F)



74S11



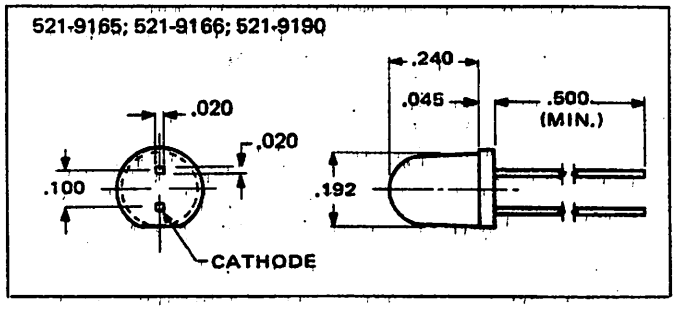
DM74S113



f_{max} = 125 MHz typ. P_D = 75 mW typ/FF
CLOCK = High to Low Transition

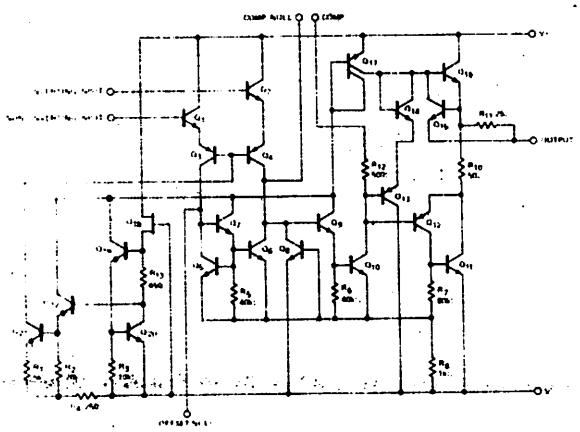
Symbol	Parameters	Minimum	Typical	Maximum
V_F	Forward Voltage @ 50 mA	–	1.8V	2.0V
BV_R	Reverse Breakdown Voltage @ 10 μA	3.0V	8.0V	–

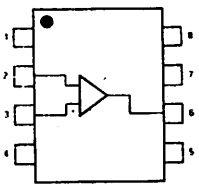
521-9165; 521-9166; 521-9190



LM301A

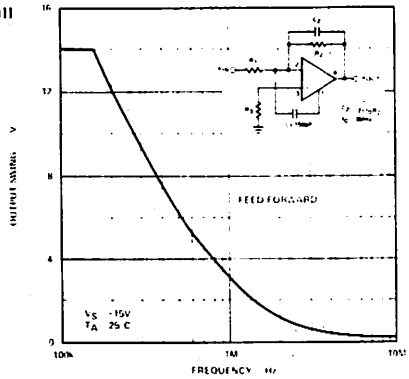
EQUIVALENT CIRCUIT





1. Freq. Comp./Offset Null
2. Inverting Input
3. Noninverting Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. Freq. Comp.

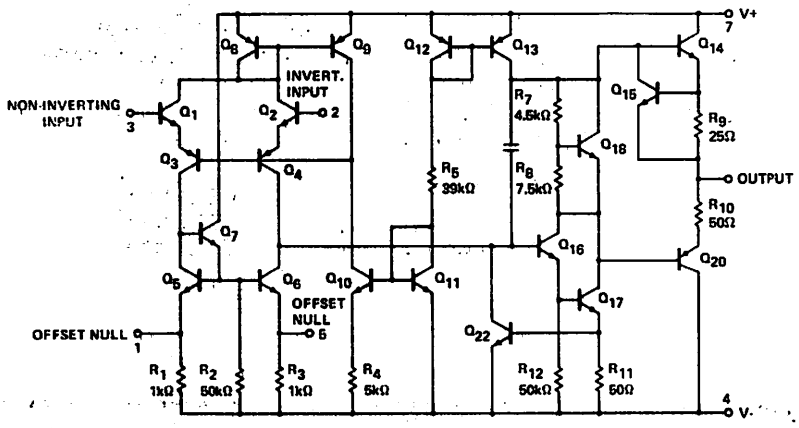
LARGE SIGNAL FREQUENCY RESPONSE

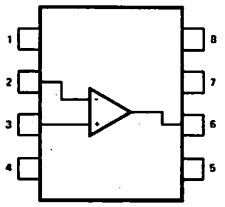


DESCRIPTION

The LM101A and LM301A are high performance operational amplifiers featuring high gain, short circuit protection, simplified compensation and excellent temperature stability.

μA741



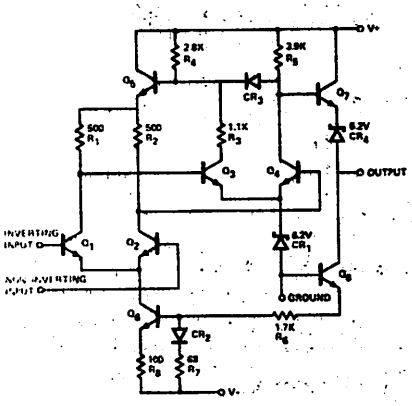


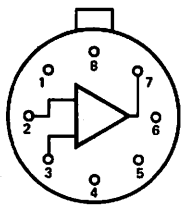
1. Offset Null
2. Inv. Input
3. Non-Inv. Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. NC

DESCRIPTION

The μA741 is a high performance operational amplifier with high open loop gain, internal compensation, high common mode range and exceptional temperature stability. The μA741 is short-circuit protected and allows for nulling of offset voltage.

μA710





1. Ground
2. Non-Inverting Input
3. Inverting Input
4. V^-
5. NC
6. NC
7. Output
8. V^+

DESCRIPTION

The μA710 is a High Speed Differential Voltage Comparator featuring low offset voltage, high sensitivity and a wide input voltage range. It is ideally suited for use as a pulse height discriminator, an analog comparator or a digital line receiver. The output structure of the μA710 is compatible with DTL, TTL and Utilogic integrated circuits.

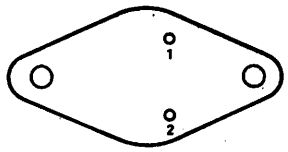
Voltage Regulators

LM309

DESCRIPTION

The LM109 and LM309 are complete 5 volt regulators fabricated on a single silicon chip. These regulators are designed for local "on card" regulation to eliminate many of the noise and ground loop problems associated with single-point regulation. They employ internal current limiting, thermal shutdown, and safe-area compensation which makes the circuitry essentially blow-out proof. If adequate heat sinking is provided, the devices can deliver output currents in excess of 200mA from the TO-5 package, and 1A from the TO-3 package. In addition to their use as fixed 5 volt regulators, these devices may be used with external components to obtain adjustable output levels. They may also be used as the power pass element in precision regulators.

K PACKAGE
(Bottom View)



1. Input
2. Output

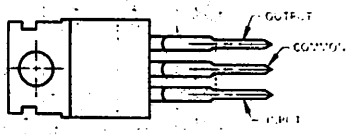
Case is connected to ground.

μA7800 SERIES

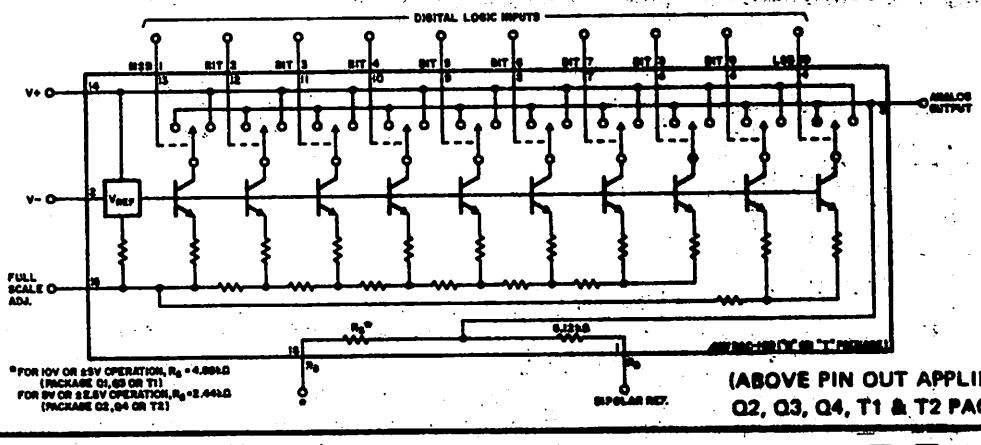
μA7815 . . . . . 15 V

GENERAL DESCRIPTION – The μA7800 series of Three-Terminal Positive Voltage Regulators are constructed using the Fairchild Planar* epitaxial process. These regulators employ internal current limiting, thermal shutdown and safe-area compensation making them essentially blow-out proof. If adequate heat sinking is provided, they can deliver over 1A output current. They are intended as fixed-voltage regulators in a wide range of applications including local, on-card regulation for elimination of noise and distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and as the power pass element in precision regulators.

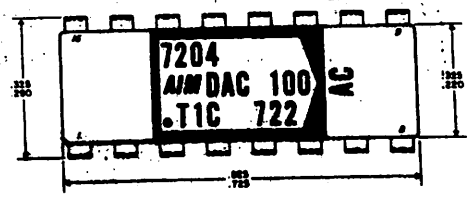
CONNECTION DIAGRAMS
TO-220 PLASTIC POWER PACKAGE
(TOP VIEW)



SIMPLIFIED SCHEMATIC AND PIN CONNECTION DIAGRAM (DUAL-IN-LINE PACKAGES)



(ABOVE PIN OUT APPLIES FOR Q1, Q2, Q3, Q4, T1 & T2 PACKAGES)



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